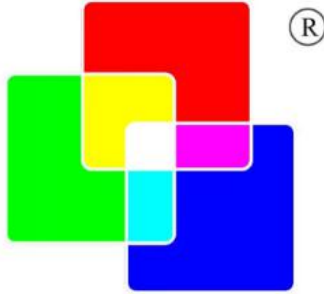


<b>PREPARED BY :</b> 制作人 ::HJW 日期: 2025-02-13	 <p><b>EASYQUICK</b></p> <p><b>TECHNOLOGY</b></p> <p>SPECIFICATION</p> <p>深圳市易快来科技股份有限公司</p>	<b>SPEC No:</b> (规格型号: ) <b>EQTA01BKI322P</b>
<b>R&amp;D APPROVED BY:</b> 审核:GJM 日期: 2025-02-13		<b>FILE No :</b> (档案编号 : ) <b>EQ2025021301</b>
<b>QC APPROVED BY:</b> 确认: WPC 日期: 2025-02-13		<b>ISSUE (日期)</b> 2025-02-13  <b>PAGE (页码)</b> 18
<b>APPLICABLE DIVISION</b> (适用范围)  <input checked="" type="checkbox"/> LCD DIVISION <input type="checkbox"/> 液晶模组		

For **800\*1280** TFT LCD Module Model No

# EQTA01BKI322P

## SPEC

**Customer side signature (客户方签名)**

部门 \ 签名	Acknowled-ge (承认人)	Date (日期)	Remarks (备注)
<b>Structure</b> (结构)			
<b>Electronics</b> (电子)			
<b>Item</b> (项目)			
<b>Quality</b> (品质)			

**EASYQUICK TECHNOLOGY**

(易快来科技)

PEC No.	MODEL No.	Revised	PAGE
EQ2025021301	EQTA01BKI322P	Ver01	1



## 1. Application (应用)

This data sheet is to introduce the specification of **EQTA01BKI322P** active matrix **16.7M** color TFT LCD module.

Main color LCD module is controlled by Driver IC **ILI9881C**.

If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.

As to basic specification of driver IC refer to the IC specification and handbook.

本规格书是为了介绍 **EQTA01BKI322P** 有源矩阵 **16.7M** 彩色 TFT LCD 模块的规格。

主彩色液晶显示模块由驱动芯片 **ILI9881C** 控制

本规范未尽事宜如有问题，双方必须认真协商解决。

驱动 IC 的基本规格参照《IC 规格书》和相关《手册》。

## 2. Construction and Outline (结构与大纲)

Construction: LCD panel, Driver (COG), FPC with electric components, **28** White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.

In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.

So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

结构:液晶面板，驱动或 COG，带电子元件的 FPC，**28** 个白光 LED 块，棱镜片，扩散器，导光器和反射器，塑料框架机械固定。

不应有可能影响显示功能的划痕、污迹、芯片、畸变等外部缺陷。

为了实现薄型模块结构，采用双面胶带固定液晶面板。由于这些胶带不能保证永久有效固定面板，LCD 面板在出厂时可能会从模块内移动。

所以在液晶模块组包装和进柜时，请务必将包装结构设计成用海绵等软材料支撑液晶面板的边缘。



### 3. Mechanical Specification (参数规格)

No.	Item	Contents	Unit
1	Screen size (屏幕尺寸)	10.1 inch	/
2	Display mode (显示模式)	Normally black	/
3	View Angle (视角)	FULL VIEW	/
4	Display format (分辨率)	800*1280	/
5	Outline Dimensions (外形尺寸)	162.50(W)×242.0(H)×4.74(D)	mm
6	Active area (显示范围)	135.36 (H)x 216.58 (V)	mm
7	Pixel size(像素)	0.1692(H)×0.1692(V)	mm
8	Interface type (接口类型)	MIPI 4 lane	/
9	Color Depth (颜色深度)	16.7M	/
10	Module power consumption (模组功耗)	TBD	mW
11	Back light type (背光类型)	LED	/
12	Driver IC (驱动 IC)	ILI9881C	/
13	Weight (重量)	TBD	g

Note 1: Not include FPCs & Bezel extrude structure.

备注 1: 不包括排线和面板构造

### 4. ABSOLUTE MAXIMUM RATINGS(绝对最高额定值)

Item	Symbol	Min.	Max.	Unit	Note
I/O logic voltage (I/O 逻辑电压)	IOVCC	-0.3	3.8	V	
Supply voltage (供电电压)	VCC	-0.3	7	V	
Operation temperature (运行温度)	Top	-10	+50	°C	
Storage temperature (储存温度)	Tst	-20	+60	°C	



## 5. ELECTRICAL CHARACTERISTICS (电气特性)

### 5.1 TFT DC CHARACTERISTICS(at Ta=25°C)

#### TFT 直流特性(at Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply input voltage (电源输入电压)	VCI	2.5	2.8	6.6	V	
I/O logic voltage (I/O 逻辑电压)	VDDI	1.65	2.8	3.6	V	
Input voltage 'H' level (输入电压高水平)	VIH	0.7VDDI	-	VDDI	mV	
Input voltage 'L' level (输入电压低水平)	VIL	0	-	0.3VDDI	mV	
Power supply current (电源电流)	Ivci	-	TBD	-	mA	
I/O logic voltage current (I/O 逻辑电压电流)	IVDDI	-	TBD	-	mA	
TFT gate on voltage (TFT门打开电压) / Input positive voltage(输入正极电压)	VSP	-	-	-	V	
TFT gate off voltage (TFT门关闭电压) / Input Negative voltage(输入负极电压)	VSN	-	-	-	V	
Analog power supply voltage (模拟电源电压)	AVDD	-	-	-	V	
TFT input common mode voltage (TFT输入共模电压)	VCOM	-	-	-	V	Note1

Note1 : The value is just the reference value. The customer can optimize the setting value by the different D-IC

Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..

备注：该值只是参考值，应用于不同的驱动芯片需要优化设定值，VCOM 必须进行调整来优化显示质量，比如串扰、对比度等



## 5. 2 LED back light (背光灯)

At main panel the back light uses 28 pcs edge light type white LED.

在背光的主面板用 28 颗白色 LED 灯

Table 4 (表 4)

Parameter (参数)	Symbol (样品)	Min. (最小值)	Typ. (标准值)	Max. (最大值)	Unit (单位)	Remark (备注)
LED Voltage (LED 电压)	VLED	18.9	21	23.1	V	
LED Current (LED 电流)	ILED	-	80	-	mA	
Power Consumption (电功率)	WLED	-	1680	-	mW	
Connection Type (Serial/Parallel/Other) 连接类型(串联/并联/其他)	7S4P LEDs					

### Note:

\*28 pcs of LED

\*Please consider Allowable Forward Current on used temperature

\*28 颗灯

\* 请考虑允许范围内的正向电流的使用温度



Backlight LED Circuit  
 $I_f=80\text{mA}; V_f=21 \pm 2.1\text{V}$

Fig.1\*Schematics drawing of lighting (绘制照明图 图.1)

## 6. Interface signals (接口信号)

### TFT Module Interface description (TFT 模块接口描述)

Pin No.	LCD 接口 pin 定义	LCD 接口说明
1	NC	NC
2	VCC(3.3V)	LCD 电源 3.3V
3	VCCIO(3.3V)	I/O 电源 3.3V
4	GND	地
5	RESET	LCM-RESET
6	NC	NC
7	GND	地
8	D0N	MIPI-D0N
9	D0P	MIPI-D0P
10	GND	地
11	D1N	MIPI-D1N
12	D1P	MIPI-D1P
13	GND	地
14	CLKN	MIPI-CLKN
15	CLKP	MIPI-CLKP
16	GND	地
17	D2N	MIPI-D2N
18	D2P	MIPI-D2P
19	GND	地
20	D3N	MIPI-D3N
21	D3P	MIPI-D3P
22	GND	地
23-24	NC	NC
25	GND	地
26-29	NC	NC
30	GND	地
31-32	LEDK	背光负极
33-38	NC	NC
39-40	LEDA	背光正极

## 7. AC CHARACTERISTICS (交流特性)

### 17.4.1. DSI Timing Characteristics

### 17.4.2. High Speed Mode – Clock Channel Timing

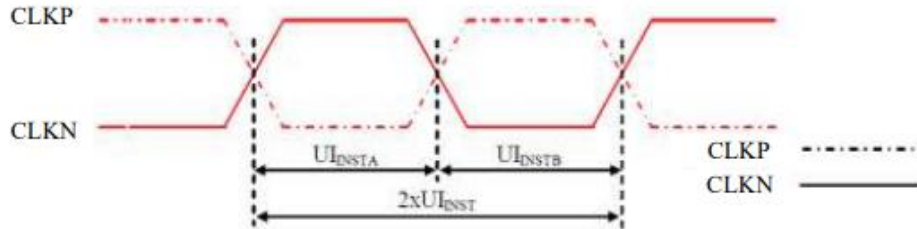


Figure 105: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	Note 2	25	ns
CLKP/N	$UI_{INSTA}, UI_{INSTB}$ (Note 1)	UI instantaneous Half	Note 2	12.5	ns

**Notes:**

1.  $UI = UI_{INSTA} = UI_{INSTB}$
2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps

### High Speed Mode – Data Clock Channel Timing

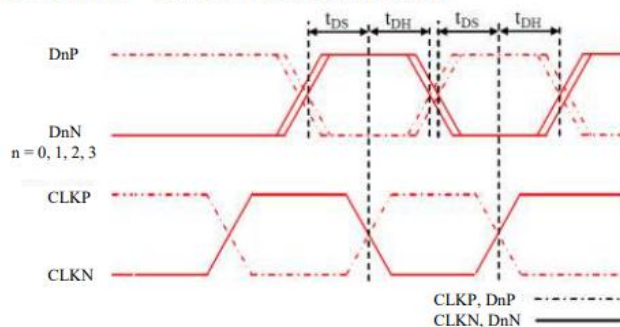


Figure 106: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N, n=0 and 1	$t_{DS}$	Data to Clock Setup time	0.15xUI	-
	$t_{DH}$	Clock to Data Hold Time	0.15xUI	-

#### 4. High Speed Mode – Rising and Falling Timings

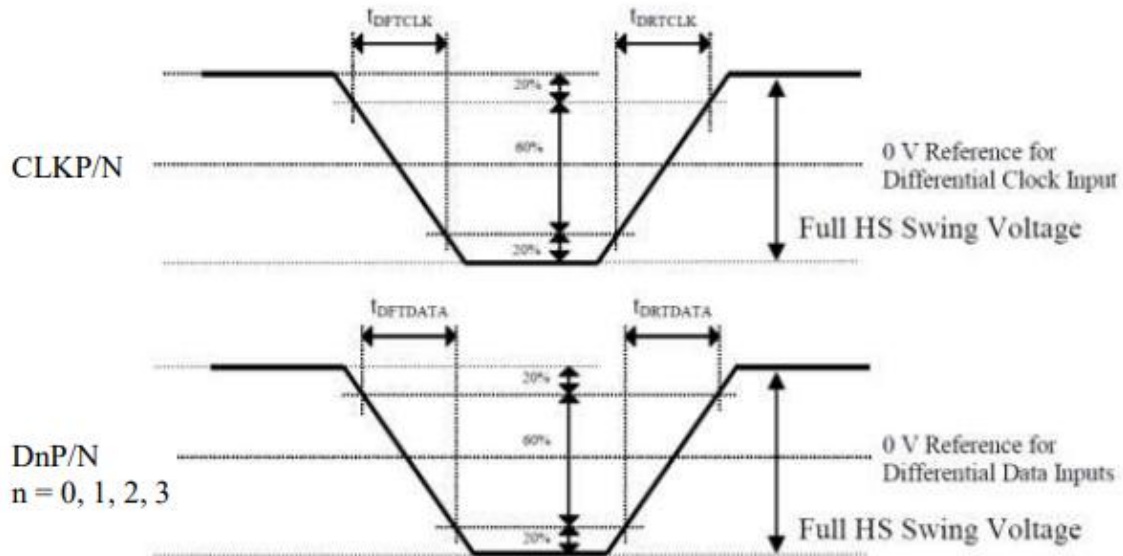


Figure 107: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	$t_{DRTCLK}$	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	$t_{DFTCLK}$	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.



### 17.4.5. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C-04) are illustrated for reference purposes below.

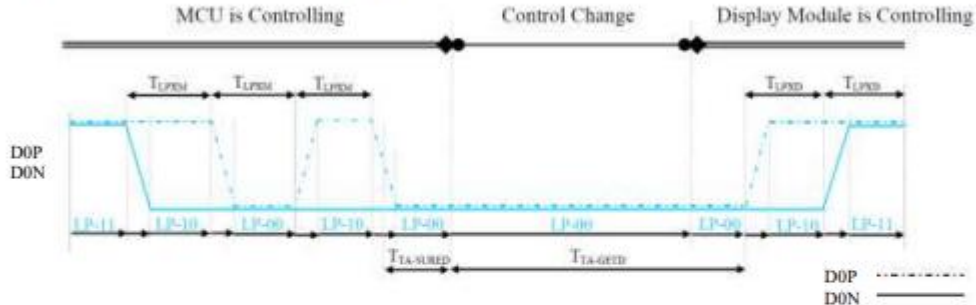


Figure 108: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C-04) to the MCU are illustrated for reference purposes below.

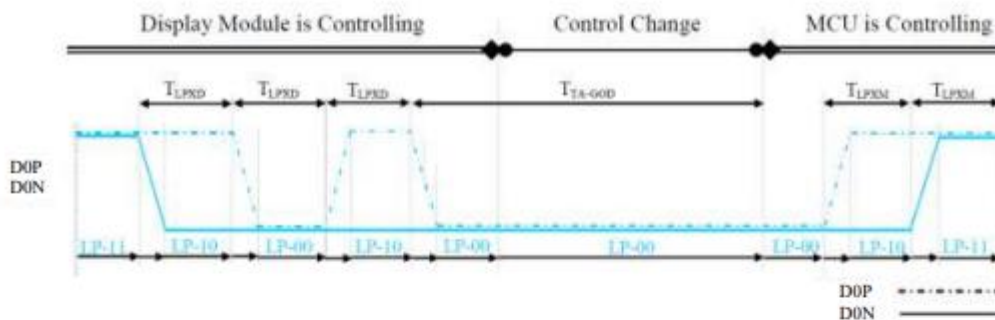


Figure 109: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	$T_{LPXM}$	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C-04)	50	75	ns
D0P/N	$T_{LPXD}$	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C-04) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C-04) starts driving	$T_{LPXD}$	$2 \times T_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C-04)	$5 \times T_{LPXD}$	ns
D0P/N	$T_{TA-G0D}$	Time to drive LP-00 after turnaround request - MCU	$4 \times T_{LPXD}$	ns

### 17.4.6. Data Lanes from Low Power Mode to High Speed Mode

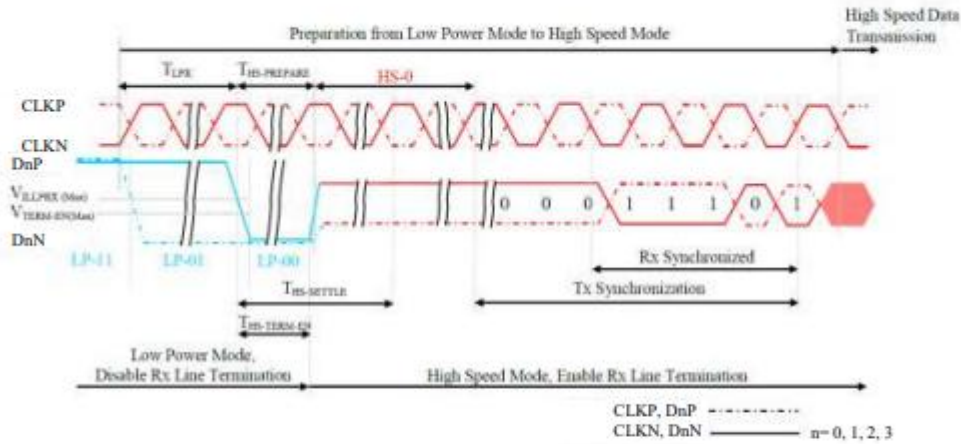


Figure 110: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{LPK}$	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	$40+4xU_I$	$85+6xU_I$	ns
DnP/N, n = 0 and 1	$T_{HS-TERMIN-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	$35+4xU_I$	ns

### 17.4.7. Data Lanes from High Speed Mode to Low Power Mode

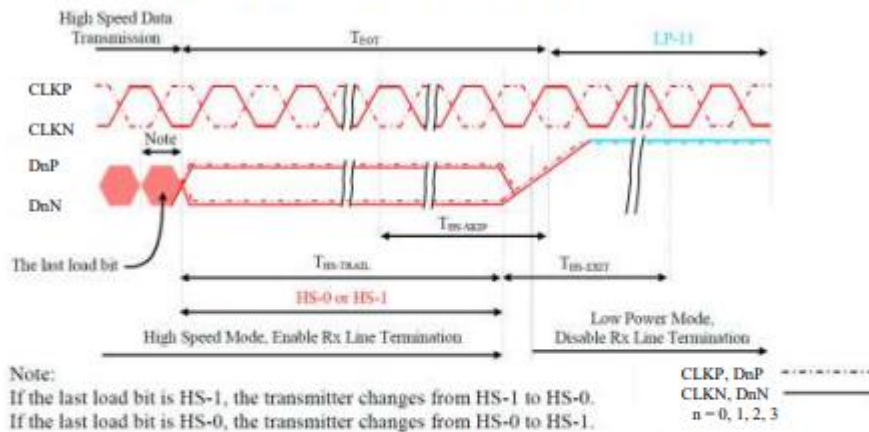


Figure 111: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SOP}$	Time-Out at Display Module (ILI9881C-04) to ignore transition period of EoT	40	$55+4xU_I$	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

### 17.4.8. DSI Clock Burst – High Speed Mode to/from Low Power Mode

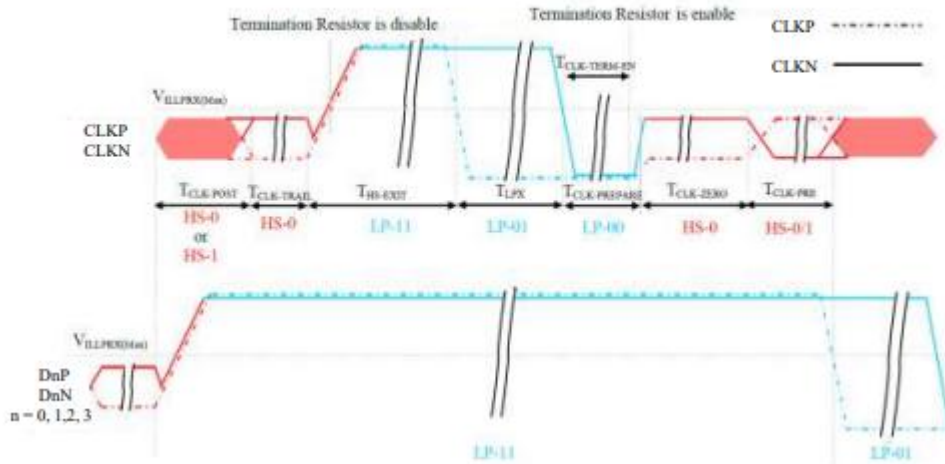
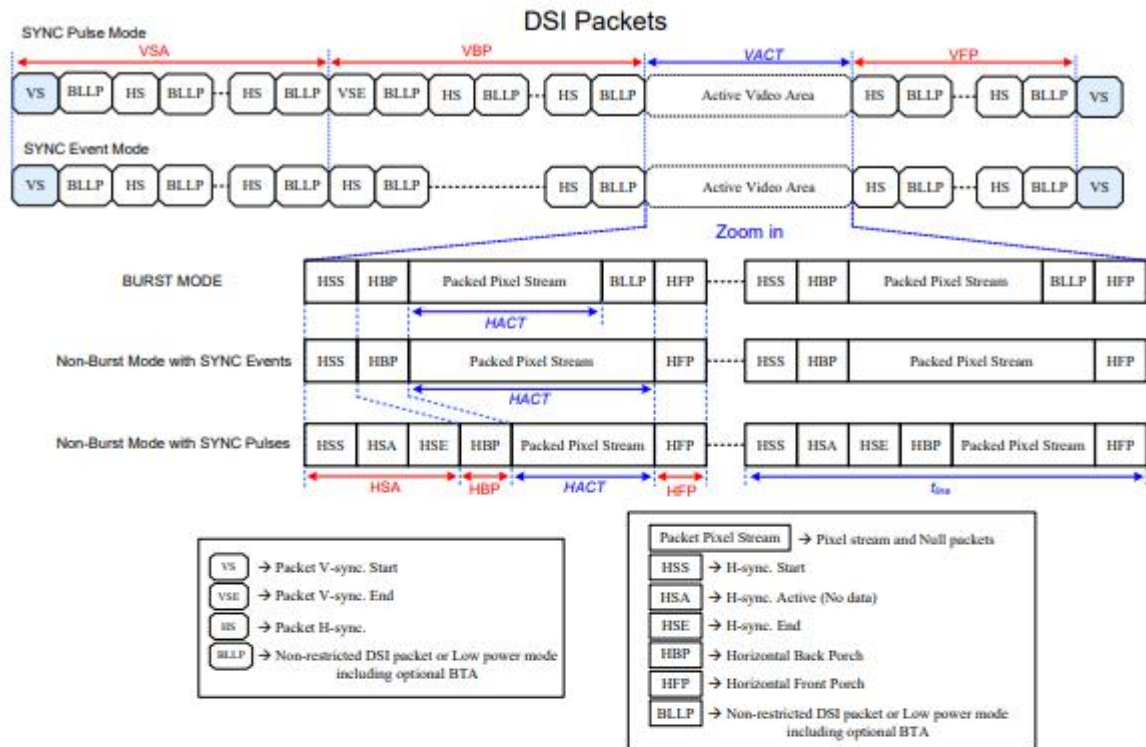


Figure 112: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	$60+52xUI$	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$8xUI$	-	ns

### 17.4.9. Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 <small>(Note 6)</small>	-	-	Line
Vertical Back Porch	VBP	14 <small>(Note 6)</small>	-	-	Line
Vertical Front Porch	VFP	8 <small>(Note 6)</small>	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR <sub>bps</sub>	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel)= (tHSA\*lane number ) / (UI\* pixel format )

HBP(pixel)= (tHBP\*lane number ) / (UI\* pixel format )

HFP(pixel)= (tHFP\*lane number ) / (UI\* pixel format )

$$\text{Frame Rate} = \frac{\text{BR}_{\text{bps}} \times \text{Lane}_{\text{num}}}{(\text{VACT} + \text{VSA} + \text{VBP} + \text{VFP}) \times (\text{HACT} + \text{HSA} + \text{HBP} + \text{HFP}) \times \text{Pixel Format}}$$

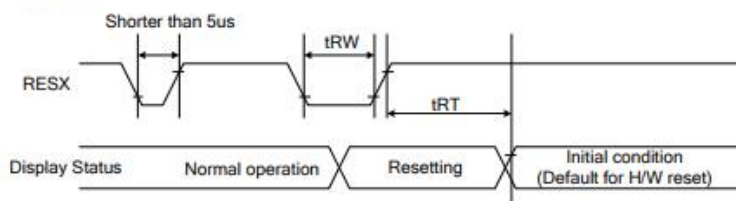
Example : BR<sub>bps</sub> = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, Lane<sub>num</sub>=4(lane), Pixel Format=24(bit).



**Note:**

1. Lane<sub>num</sub>: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to "4.1DSI System Interface".
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting : 2 data lanes : 50~60 Hz / 3 data lanes : 50~70 Hz / 4 data lanes : 50~70 Hz.
5. Please reference to "Table 39: Limited Clock Channel Speed".
6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

**17.4.10. Reset Timing**



**Figure 113: Reset Timing**

**Table 47: Reset Timing**

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1.5) 120 (note 1.6.7)	mS

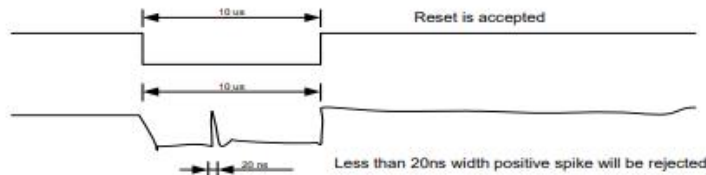
**Notes:**

1. The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.

**Table 48: Reset Descript**

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:



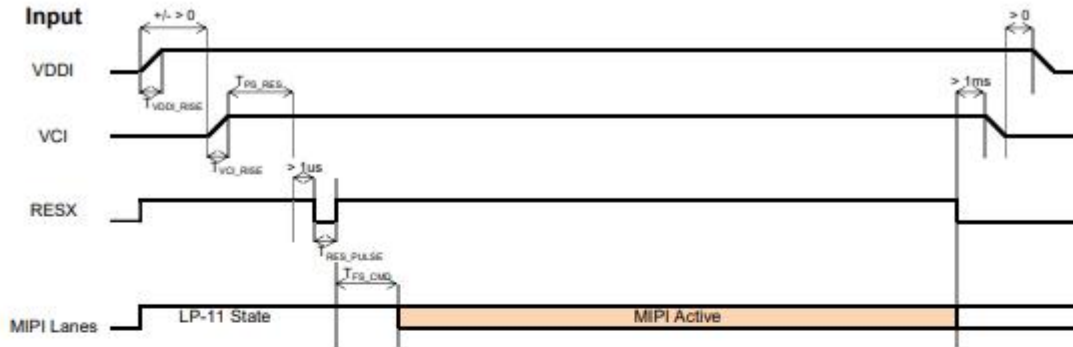
**Figure 114: Positive Noise Pulse during Reset Low**

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

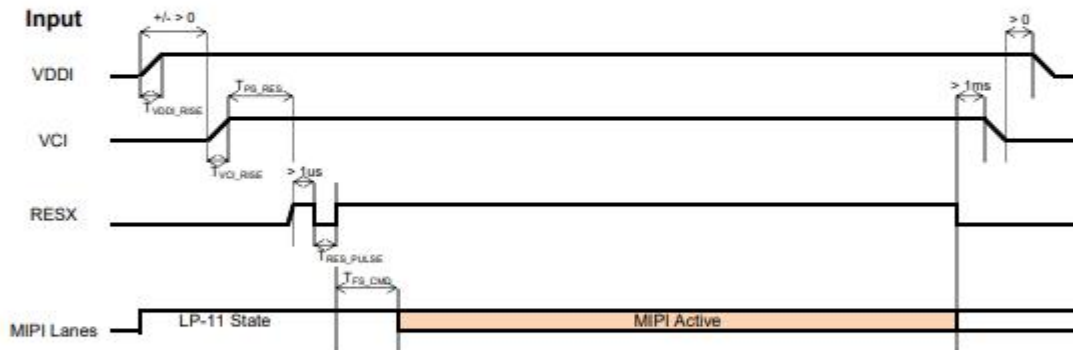
## 8. POWER SEQUENCE (电源时序)

### 11.1.2. Power Mode 3

#### Case A:



#### Case B:



Symbol	Characteristics	Min.	Typ.	Max.	Units
$T_{VDDI\_RISE}$	VDDI Rise time	10	-	-	us
$T_{VCI\_RISE}$	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
$T_{PS\_RES}$	VDDI/VCI on to Reset high	5	-	-	ms
$T_{RES\_PULSE}$	Reset low pulse time	10	-	-	us
$T_{FS\_CMD}$	Reset to first command	10	-	-	ms

Figure 93: Power on/off sequence with Power Mode 3

## 9. Optical Characteristics (光学特征)

Item 项目		Symbol (样品)	Condition (条件)	Min. (最小值)	Typ.(标准值)	Max. (最大值)	Unit (单位)	Remark (备注)
Response time (响应时间)	Rise (上升)	Tr +Tf	$\theta=0^\circ$	-	30	-	ms	Note 1 FIG.1
	+Fall (下降)							
Luminance (亮度)		Br	$\theta=0^\circ$	400	450	-	Cd/m <sup>2</sup>	Note 3 FIG.2
Luminance uniformity (亮度均匀性)		YU	$\theta=0^\circ$	80	-	-	%	Note 4 FIG.2
Contrast ratio (对比度)		CR	$\theta=0^\circ$	800	1000	-	-	Note 2 FIG.2
Viewing angle(with Polarizer) (视角)	Top (顶部)	CR $\geq$ 10		75	80	-	degree	Note 6 FIG.3
	Bottom (底部)			75	80	-		
	Left (左边)			75	80	-		
	Right (右边)			75	80	-		
White Chromaticity (白色色度)		X	CIE	-0.03	0.30	+0.03	-	Note 5 FIG.2 CIE1931
		Y		-0.03	0.30	+0.03	-	
NTSC (色彩饱和度)			-	52	-	-	%	Note 5 FIG.2

### Note1. Definition of response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time ( $T_{ON}$ ) is the time between photo detector output intensity changed from 90% to 10%.

And fall time ( $T_{OFF}$ ) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

### Note2. Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula.

For more information see FIG.2.

Contrast ratio=  $\frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$

Measured at the center area of the LCD



**Note3. Definition of surface luminance**

Surface luminance is the luminance with all pixels displaying white.  
For more information see FIG.2.

$L_v$  = Average Surface Luminance with all white pixels (P1,P2,P3, ..... ,Pn)

**Note4. Definition of luminance uniformity**

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

$$Y_u = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

**Note5. Definition of color chromaticity (CIE1931)**

CIE (x,y) chromaticity, The x,y value is determined by screen active area center position P5. For more information see FIG.2.

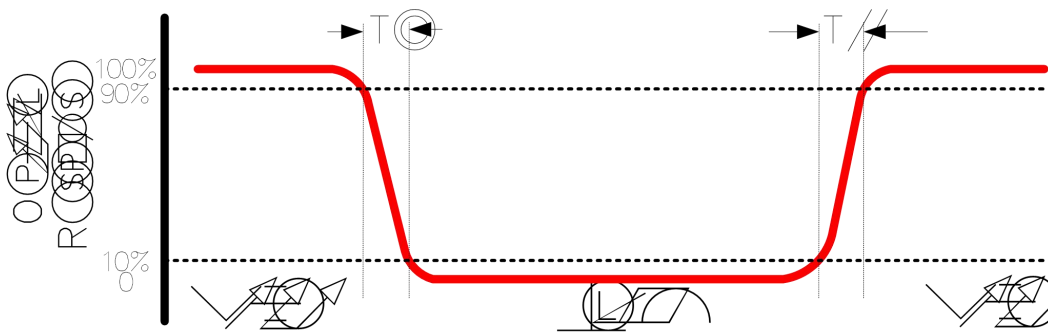
**Note6. Definition of viewing angle**

Viewing angle is the angle at which the contrast ratio is greater than 10. angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.

For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE, the testing data is base on TOPCON's BM-5 or BM-7 photo detector or compatible.

**FIG.1. The definition of response Time**



**FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity**

H,V : Active area

Light spot size  $\varnothing = 1.5\text{mm}$  (BM-7) 50cm distance or compatible distance from the LCM surface to detector lens.

Test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-7 or compatible ,see Figure b.

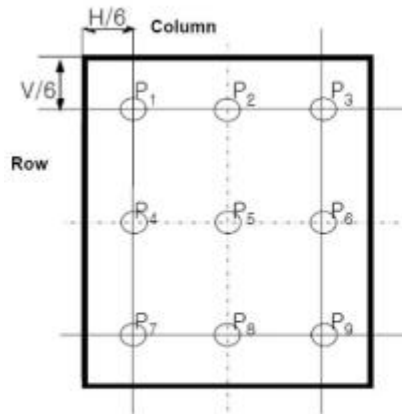


Figure a

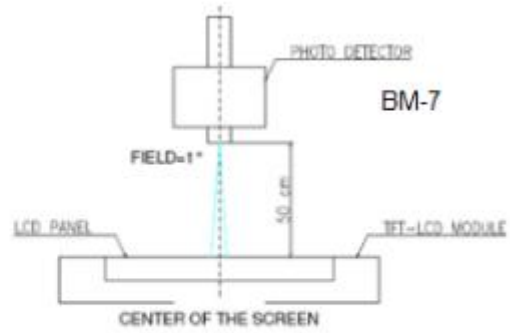
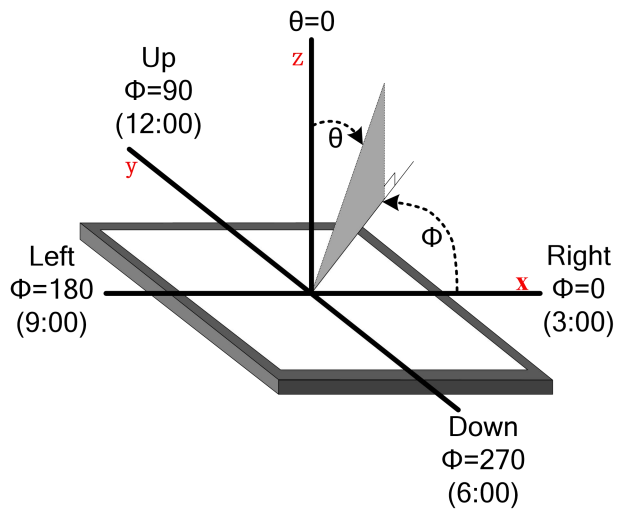
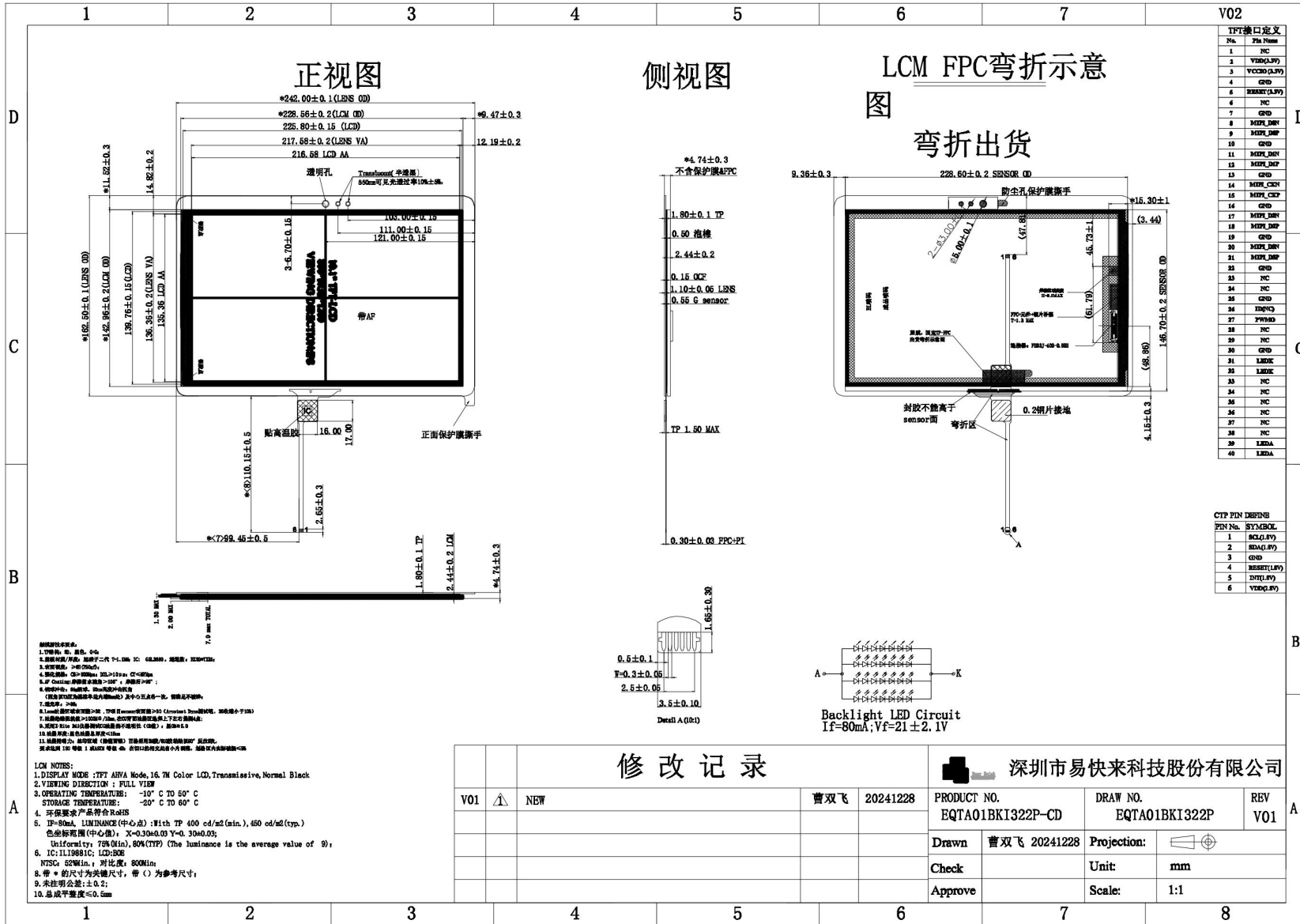


Figure b

**FIG.3. The definition of viewing angle**



# 10.LCD Module Outline dimensions (模组外形图)



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EQ2025021301	EQTA01BK1322P	Ver01	17

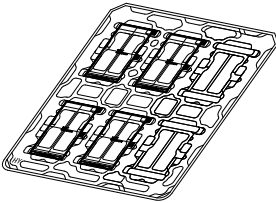
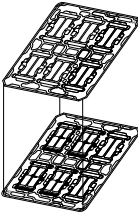

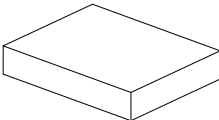
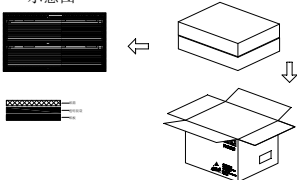
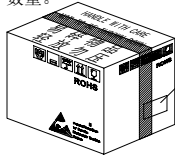
PEC No.	MODEL No.	Revised	PAGE
EQ2025021301	EQTA01BKI322P	Ver01	18



## 11. Packaging Specification (包装规格)

- 1.1 Package quantity in one Box : TBD PCS
- 1.2 Box Size : TBD mm \* TBD mm \* TBD mm
- 1.3 1 BOX = TBD CARTON
- 1.4 1 CARTON = TBD (Full tray) + 1 (dummy / top tray) = TBD tray
- 1.5 1 TRAY = TBD PCS LCM

注：此为示意图

<p>(1) 模块平放入吸塑盘内, 每盘放6PCS产品</p> 	<p>(2) 吸塑盘交叉叠放</p> 	<p>(3) 十盘加一个空盘共10x6=60pcs 吸塑盘交叉叠放后用胶袋和胶 纸打包</p>  <p style="text-align: right;">叠放次序 B C A C B C A</p>
<p>(4) 真空包装 将打包好的产品装进包装袋并抽真空密封,</p> 	<p>(5) 产品装箱 先在纸箱底下放一个纸板, 让后放一小包产品进去, 在放一个纸板在上面, 最后在放一个纸板在上面, 二包叠加装箱</p> <p>示意图</p> 	<p>(6) 封箱 外箱标签中须体现供应 商名称、EQ料号及包装 数量。</p>  <p style="text-align: right;">外箱标签贴于侧面</p> <p>数量: 2x60=120 PCS/箱</p>