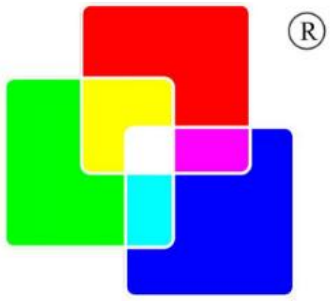
PREPARED BY : 制作人:CLM 日期：2026-01-26	 **EASYQUICK TECHNOLOGY** SPECIFICATION 深圳市易快来科技股份有限公司	SPEC No：（规格型号：） **EQT686BKV541L**
R&D APPROVED BY: 审核:GJM 日期：2026-01-26		FILE No ：（档案编号 ：） **EQ2026012601** ISSUE（日期） **2026-01-26** PAGE（页码） **19**
QC APPROVED BY: 确认：WJG 日期：2026-01-26		APPLICABLE DIVISION （适用范围） ■LCD DIVISION ■液晶模组

For **480*1280**TFT LCD Module Model No

EQT686BKV541L
SPEC

Customer side signature（客户方签名）			
签名 / 部门	Acknowled-ge（承认人）	Date（日期）	Remarks（备注）
Structure（结构）			
Electronics（电子）			
Item（项目）			
Quality（品质）			

EASYQUICK TECHNOLOGY

（易快来科技）

1. Application（应用）

This data sheet is to introduce the specification of EQT686BKV541L active matrix 16.7M color TFT LCD module.
Main color LCD module is controlled by Driver IC NV3051F.
If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.
As to basic specification of driver IC refer to the IC specification and handbook.

本规格书是为了介绍 EQT686BKV541L 有源矩阵 16.7M 彩色 TFT LCD 模块的规格。
主彩色液晶显示模块由驱动芯片 NV3051F 控制。
本规范未尽事宜如有问题，双方必须认真协商解决。
驱动 IC 的基本规格参照《IC 规格书》和相关《手册》

2. Construction and Outline （结构与大纲）

Construction: LCD panel, Driver (COG), FPC with electric components, 12 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.
There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.
In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.
So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

结构:液晶面板，驱动或 COG，带电子元件的 FPC, 12 个白光 LED 块，棱镜片，扩散器，导光器和反射器，塑料框架机械固定。
不应有可能影响显示功能的划痕、污迹、芯片、畸变等外部缺陷。
为了实现薄型模块结构，采用双面胶带固定液晶面板。由于这些胶带不能保证永久有效固定面板，LCD 面板在出厂时可能会从模块内移动。
所以在液晶模块组包装和进柜时，请务必将包装结构设计成用海绵等软材料支撑液晶面板的边缘。

3. Mechanical Specification（参数规格）

No.	Item	Contents	Unit
1	Screen size（屏幕尺寸）	6.86	inch
2	Display mode（显示模式）	Normally black	/
3	View Angle（视角）	FULL VIEW	/
4	Display format（分辨率）	480×RGB×1280	/
5	Outline Dimensions（外形尺寸）	66.8(W)×181.2(H)×4.7(D)	mm
6	Active area（ 显示范围）	60.19(H)×160.51(V)	mm
7	Cover Glass View area（盖板 VA）	--	mm
8	Interface type（接口类型）	MIPI	/
9	Color Depth（颜色深度）	16.7M	/
10	Module power consumption（模组功耗）	TBD	W
11	Back light type（背光类型）	LED	/
12	Driver IC（驱动 IC）	**NV3051F**	/
13	Weight（重量）	TBD	G

Note 1: Not include FPCs & Bezel extrude stucture.

备注 1: 不包括排线和面板构造

4. ABSOLUTE MAXIMUM RATINGS(绝对最高额定值)

Item	Symbol	Min.	Max.	Unit	Note
Power supply input voltage for TFT（TFT 电源输入电压）	VDD	-0.3	+6.6	V	
I/O logic voltage（I/O 逻辑电压）	VDDI	-0.3	+4.5	V	
Operation temperature（运行温度）	Top	-20	+70	°C	
Storage temperature（储存温度）	Tst	-30	+80	°C	

5. ELECTRICAL CHARACTERISTICS（电气特性）

5.1 TFT DC CHARACTERISTICS(at Ta=25°C)

TFT 直流特性(at Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply input voltage（电源输入电压）	VDD	2.5	2.8	6.0	V	
I/O logic voltage（I/O 逻辑电压）	VDDIO	1.65	1.8	3.6	V	
Input voltage 'H' level（输入电压高水平）	VIH	0.7IOVCC	-	IOVCC	V	
Input voltage 'L' level（输入电压低水平）	VIL	VSS	-	IOVCC	V	
Power supply current （电源电流）	IVDD	-	TBD	-	mA	
I/O logic voltage current （I/O 逻辑电压电流）	IVDDIO	-	TBD	-	mA	
TFT gate on voltage （TFT门打开电压）/ Input positive voltage(输入正极电压）	VGH	-	-	-	V	
TFT gate off voltage （TFT门关闭电压）/ Input Negative voltage(输入负极电压）	VGL	-	-	-	V	
Analog power supply voltage（模拟电源电压）	AVDD	-	-	-	V	
TFT input common mode voltage （TFT输入共模电压）	VCOM	-	-	-	V	Note1

Note1 : The value is just the reference value. The customer can optimize the setting value by the different D-IC

Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..

备注：该值只是参考值，应用于不同的驱动芯片需要优化设定值，VCOM 必须进行调整来优化显示质量，比如串扰、对比度等

5. 2 LED back light（背光灯）

At main panel the back light uses 12 pcs edge light type white LED.
在背光的主面板用 12 颗白色 LED 灯

Table 4（表 4）

Parameter（参数）	Symbol（样品）	Min.（最小值）	Typ.（标准值）	Max.(最大值)	Unit（单位）	Remark（备注）
LED Voltage（LED 电压）	VLED	8.8	9.6	10.4	V	
LED Current（LED 电流）	ILED	-	140	-	mA	
Power Consumption（电功率）	WLED	-	1344	-	mW	
Connection Type(Serial/Parallel/Other) 连接类型(串联/并联/其他)		3S4P LEDs				

Note:

*12 pcs of LED

*Please consider Allowable Forward Current on used temperature

*12 颗灯

* 请考虑允许范围内的正向电流的使用温度

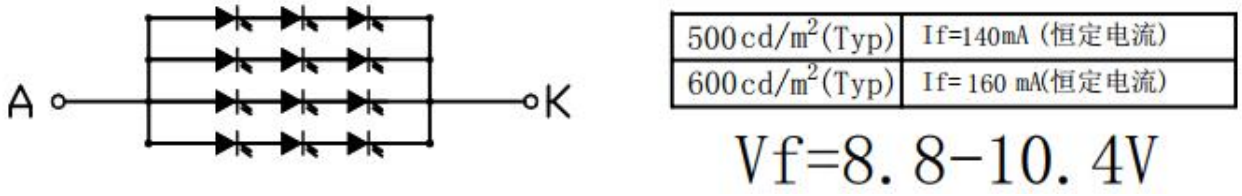


Fig.1*Schematics drawing of lighting （绘制照明图 图.1）

6. Interface signals（接口信号）

TFT Module Interface description（TFT 模块接口描述）

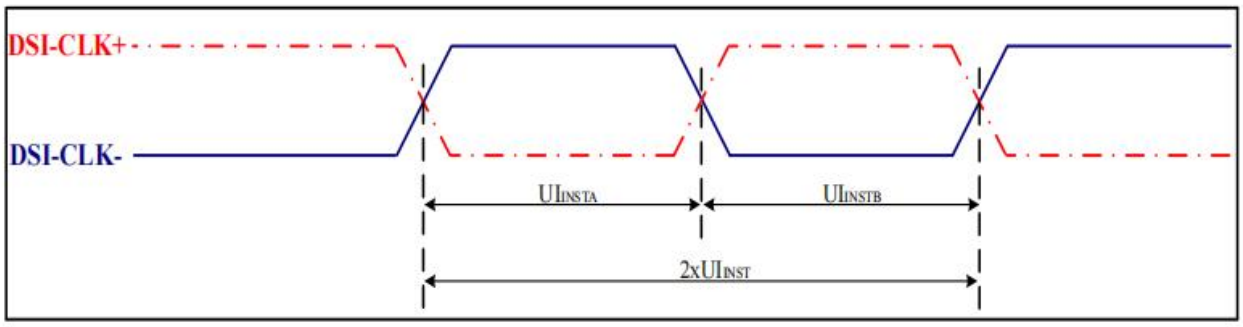
Interface No.	Name	I/O or connect to	Description
1	GND	P	Ground
2	D0P	I	MIPI-DSI data Lane 0 positive-end input pin
3	D0N	I	MIPI-DSI data Lane 0 negative-end input pin
4	GND	P	Ground
5	D1P	I	MIPI-DSI data Lane 1 positive-end input pin
6	D1N	I	MIPI-DSI data Lane 1 negative-end input pin
7	GND	P	Ground
8	CLKP	I	MIPI-DSI clock Lane positive-end input pin
9	CLKN	I	MIPI-DSI clock Lane negative-end input pin
10	GND	P	Ground
11	D2P	I	MIPI-DSI data Lane 2 positive-end input pin
12	D2N	I	MIPI-DSI data Lane 2 negative-end input pin
13	GND	P	Ground
14	D3P	I	MIPI-DSI data Lane 3 positive-end input pin
15	D3N	I	MIPI-DSI data Lane 3 negative-end input pin
16-17	GND	P	Ground
18-19	VCC-1V8	P	External logic voltage input voltage
20-23	NC	/	NC
24	RSTB	I	LCD reset pin
25-26	NC	/	NC
27	GND	P	Ground
28-29	K	P	Power for LED backlight(Cathode)
30	GND	P	Ground
31	NC	/	NC
32-33	GND	P	Ground
34	NC	/	NC
35-36	A	P	Power for LED backlight(Anode)
37	GND	P	Ground
38-39	VDD-3.3V	P	External analog voltage input voltage
40	NC	/	NC

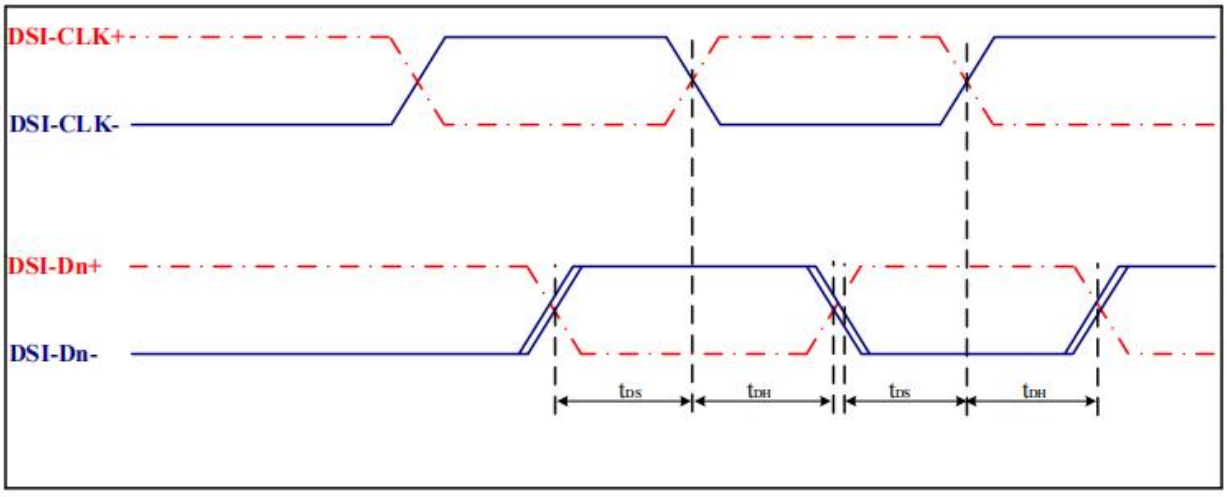
7. AC CHARACTERISTICS（交流特性）

7.1 MIPI Interface Characteristics:

High Speed Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2Xui_{inst}$	Double UI instantaneous	2.22	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	1.11	-	12.5	ns
DSI-Dn+/-	T_{ds}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	T_{dh}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	T_{drtclk}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$T_{drtdata}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	T_{dftclk}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$T_{dftdata}$	Differential fall time for data	150	-	0.3UI	ps





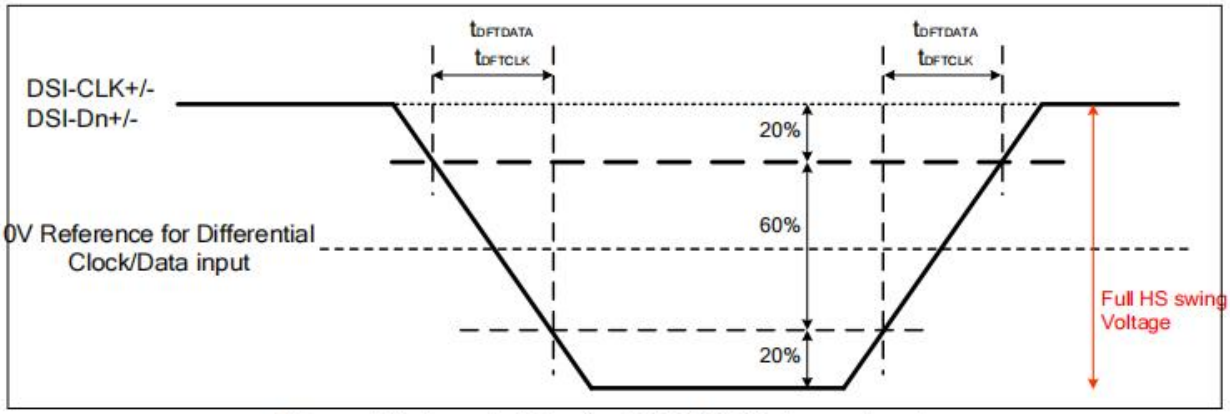


Figure: AC characteristics for MIPI-DSI High speed mode

7.2 Lowe Power Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI- D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Modulen MPU	58	-	-	ns
DSI- D0+/-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2XTLPXD	ns
DSI- D0+/-	TTA-GETD	Time to drive LP-00 by display module	5XTLPXD	-	-	ns
DSI- D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request – MPU	4XTLPXD	-	-	ns
DSI- D0+/-	Ratio TLPX	Ratio of TLPXM / TLPXD between MCU and display module	2/3	-	3/2	

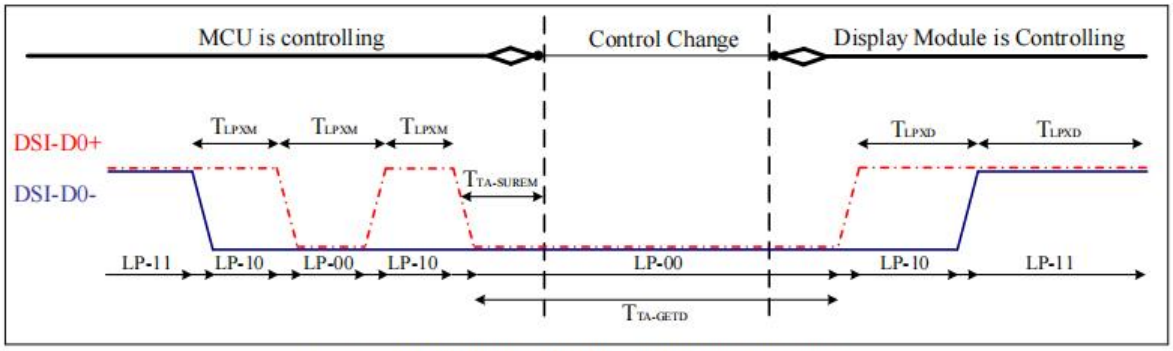


Figure: BTA from the MCU to the Display Module

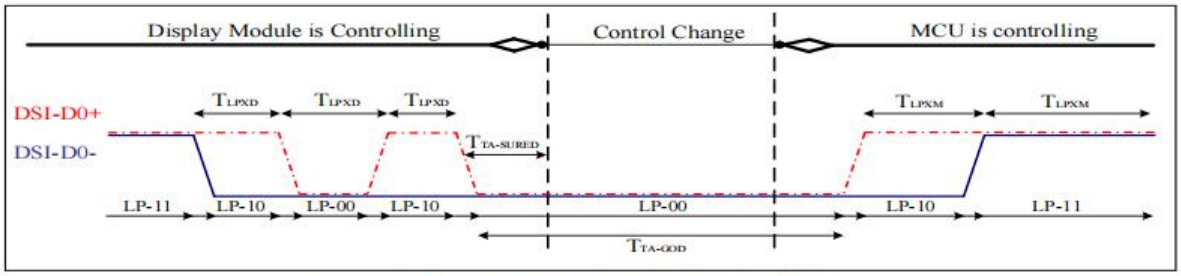


Figure: BTA from the Display Module to the MCU

7.3 DSI Bursts Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	TLPX	Length of any low-power state period	50	-	-	ns
DSI- Dn+/-	THS- PREPARE	Time to drive LP-00 to prepare for HS transmission	40ns+4UI	-	85ns+6UI	ns
DSI- Dn+/-	THS-PREPARE+THS-ZERO	THS-PREPARE+time to drive HS-0 before the sync sequence	145ns+10UI	-	-	ns
DSI- Dn+/-	TD-TERM- EN	Time to enable Data Lane receiver line termination measured from when Dn crosses VIL(max)	Time for Dn to reach VTERM-EN	-	35ns+4UI	ns
DSI- Dn+/-	THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4UI	ns
DSI- Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI- Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns
DSI- Dn+/-	TeoT	Time from start of THS-TRAIL period to start of LP-11 state	-	-	105ns+12UI	ns

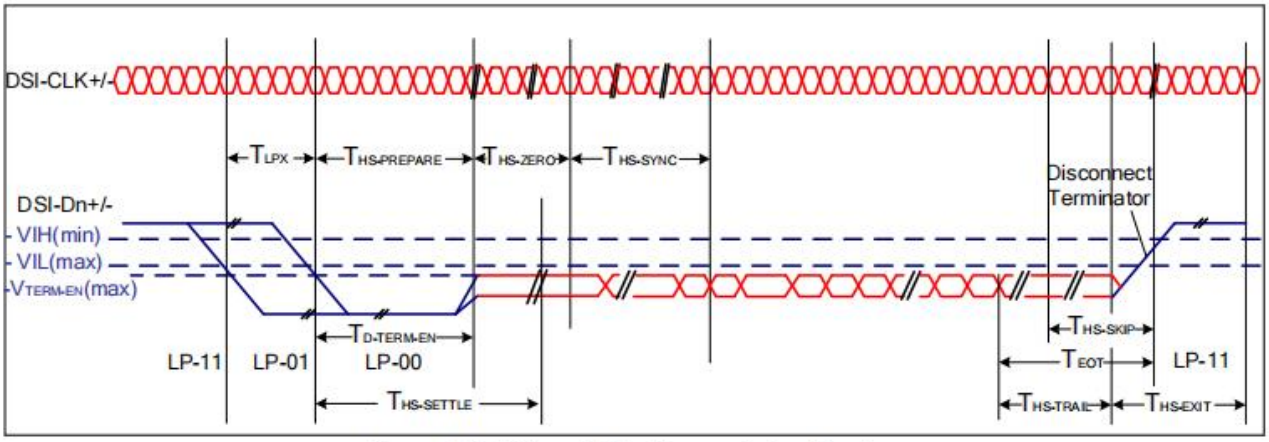


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	TCLK-POST	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns+52UI	-	-	ns
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	TCLK-TERM- EN	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach VTERM-EN	-	38	ns
DSI- CLK+/-	TCLK-PREPARE +TCLK-ZERO	TCLK-PREPARE + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI- CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	TeoT	Time from start of TCLK-TRAIL period to start of LP-11 state	-	-	105ns+ 12UI	ns

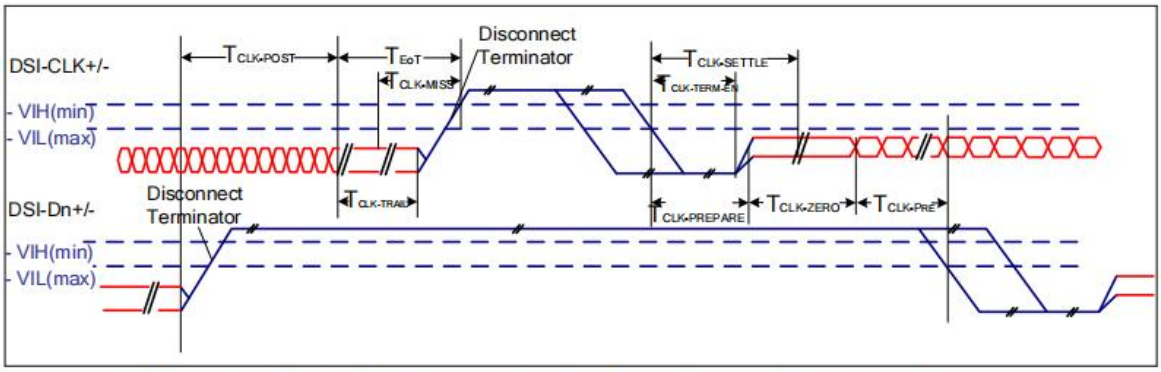
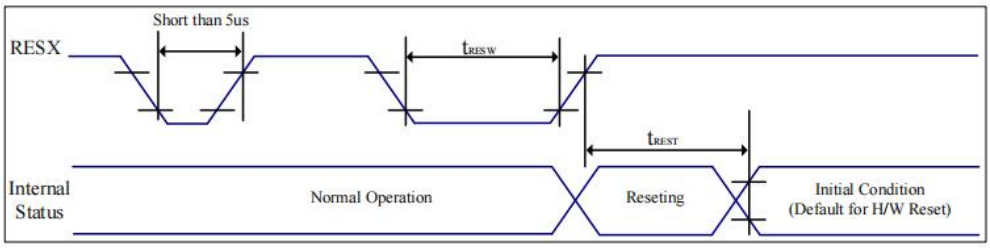


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

7.4 Reset TIming



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V,Ta = -30°C to 85°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
T_{resw}	*1) Reset low pulse width	RESX	10	-	-	-	us
T_{rest}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

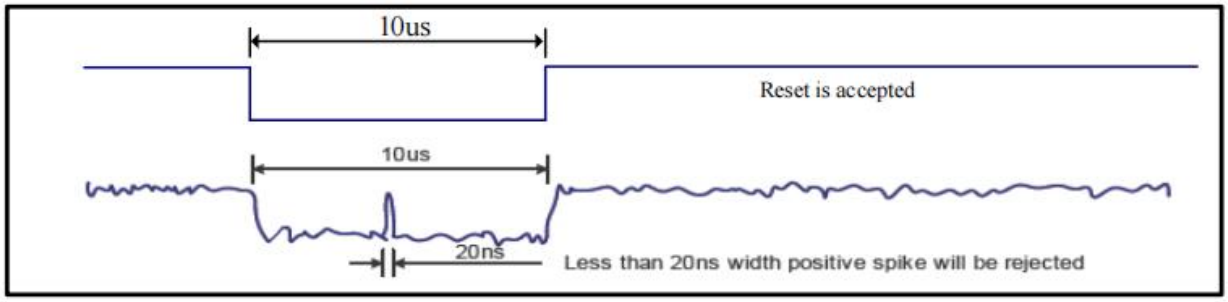
Note 1: Due to an electrostatic discharge on RESX line,spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode) , then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (Trest) which lasted 5ms.The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

8. POWER SEQUENCE（电源时序）

IOVCC and VCI can be applied in any order. IOVCC and VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, IOVCC or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command.

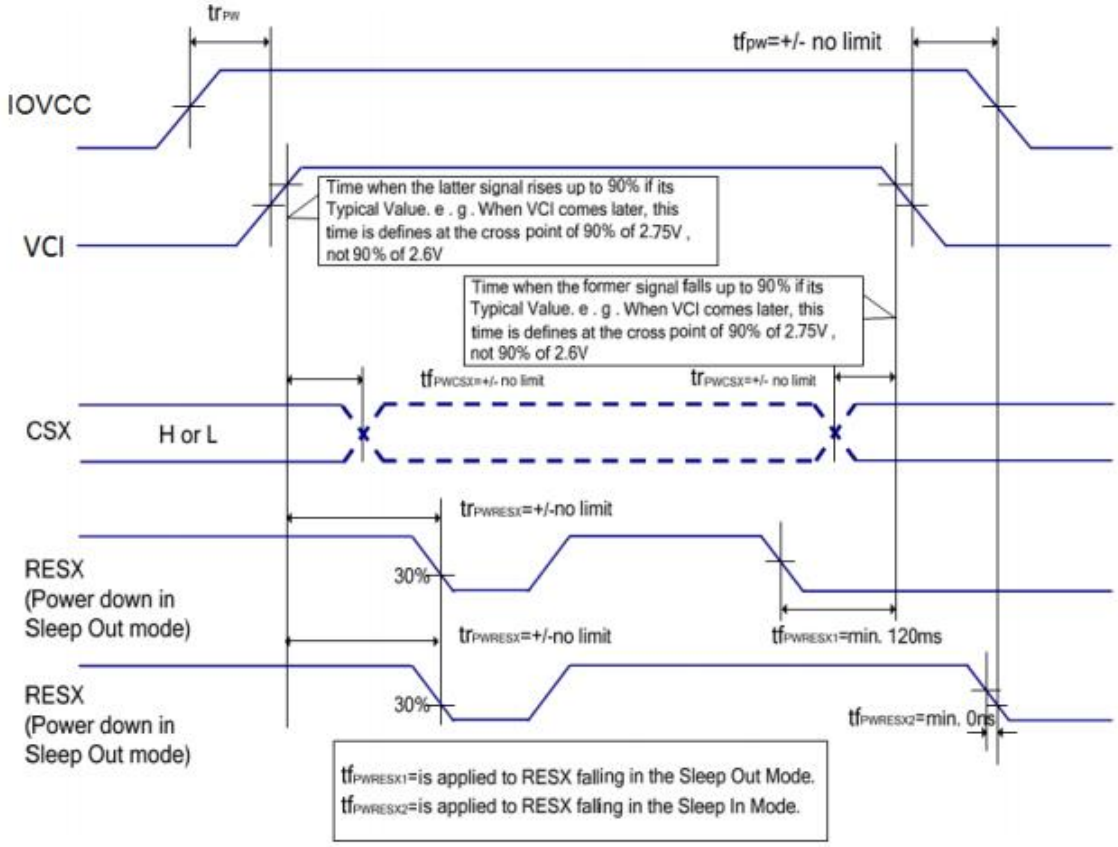
Also between receiving Sleep In command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

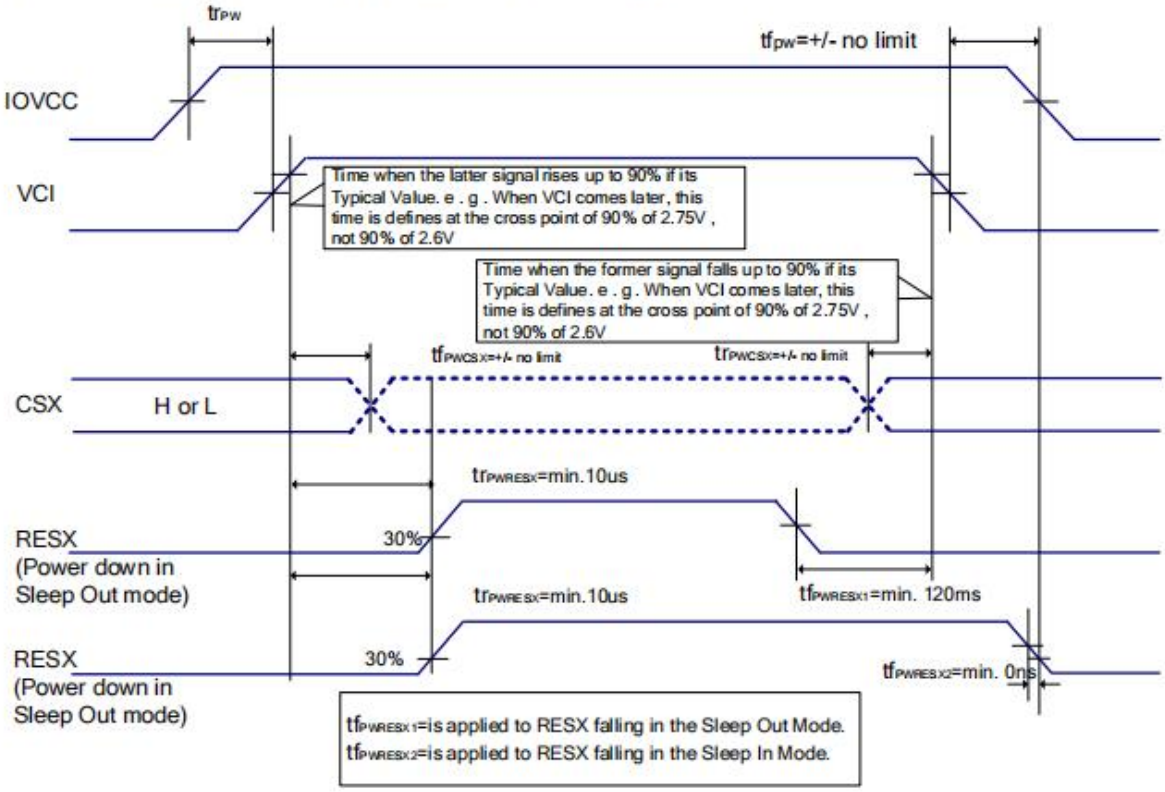
6.5.1. Case 1 – RESX line is held high or unstable by host at power on

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



6.5.2. Case 2 – RESX line is held low or unstable by host at power on

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10sec after both VCI and IOVCC have been applied.



6.5.3. Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface.

At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

9. Optical Characteristics（光学特征）

Item 项目		Symbol（样品）	Condition（条件）	Min.（最小值）	Typ.（标准值）	Max.（最大值）	Unit（单位）	Remark（备注）
Response time（响应时间）	Rise（上升）+Fall（下降）	Tr +Tf	θ=0°	-	35	40	ms	Note 1 FIG.1
Luminance（亮度）		Br	θ=0°	450	500	-	Cd/m^2	Note 3 FIG.2
Luminance uniformity（亮度均匀性）		YU	θ=0°	-	80	-	%	Note 4 FIG.2
Contrast ratio（对比度）		CR	θ=0°	1000	1500	-	-	Note 2 FIG.2
Viewing angle(with Polarizer)（视角）	Top（顶部）		CR≥10	75	85	-	degree	Note 6 FIG.3
	Bottom（底部）			75	85	-		
	Left（左边）			75	85	-		
	Right（右边）			75	85	-		
White Chromaticity（白色色度）		X	CIE	0.25	0.28	0.31	-	Note 5 FIG.2 CIE1931
		Y		0.26	0.29	0.32	-	
NTSC（色彩饱和度）			-	65	70	-	%	Note 5 FIG.2

Note1. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state.Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%.

And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

Note2.Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula.

For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

Measured at the center area of the LCD

Note3.Definition of surface luminance

Surface luminance is the luminance with all pixels displaying white.

For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note4.Definition of luminance uniformity

The luminance uniformity in surface luminance is det-ermined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$Yu = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.

For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON's BM-5or BM-7 photo detector or compatible.

FIG.1. The definition of response Time

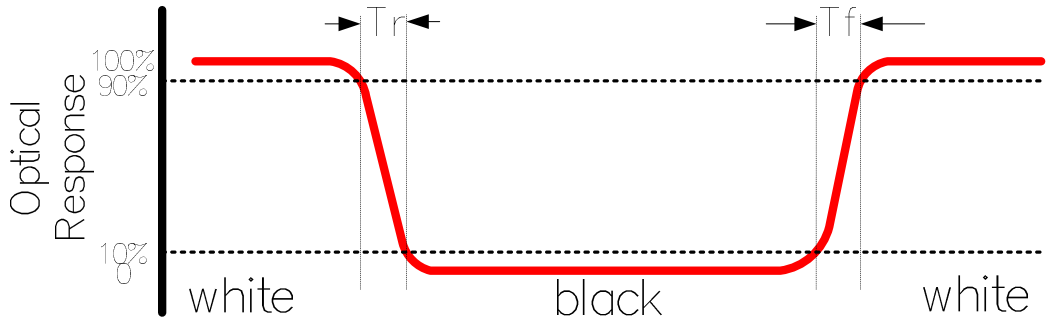


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

H,V : Active area

Light spot size ∅=1.5mm (BM-7)50cm distance or compatible distance from the LCM surface to detector lens.

Test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-7 or compatible ,see Figure b.

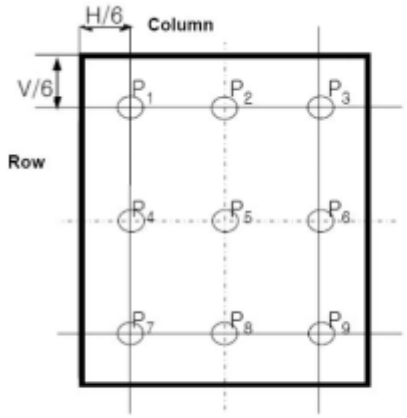


Figure a

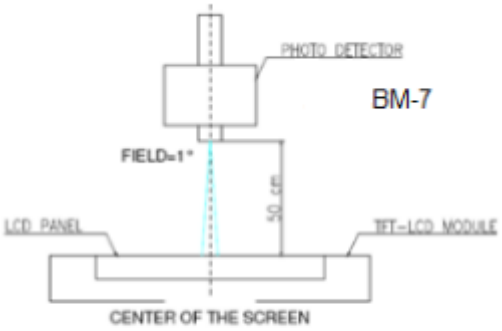
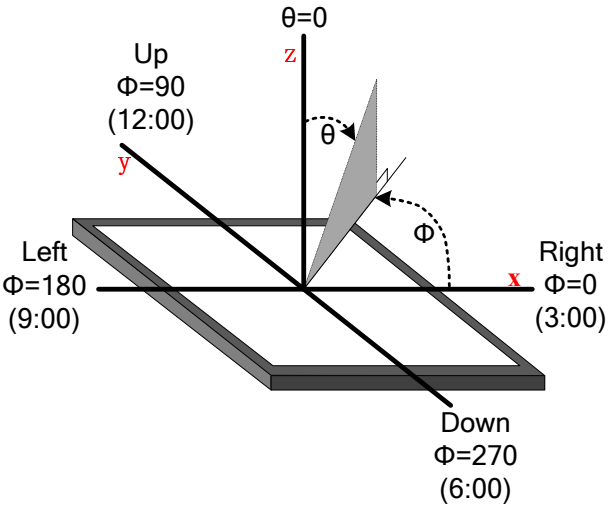
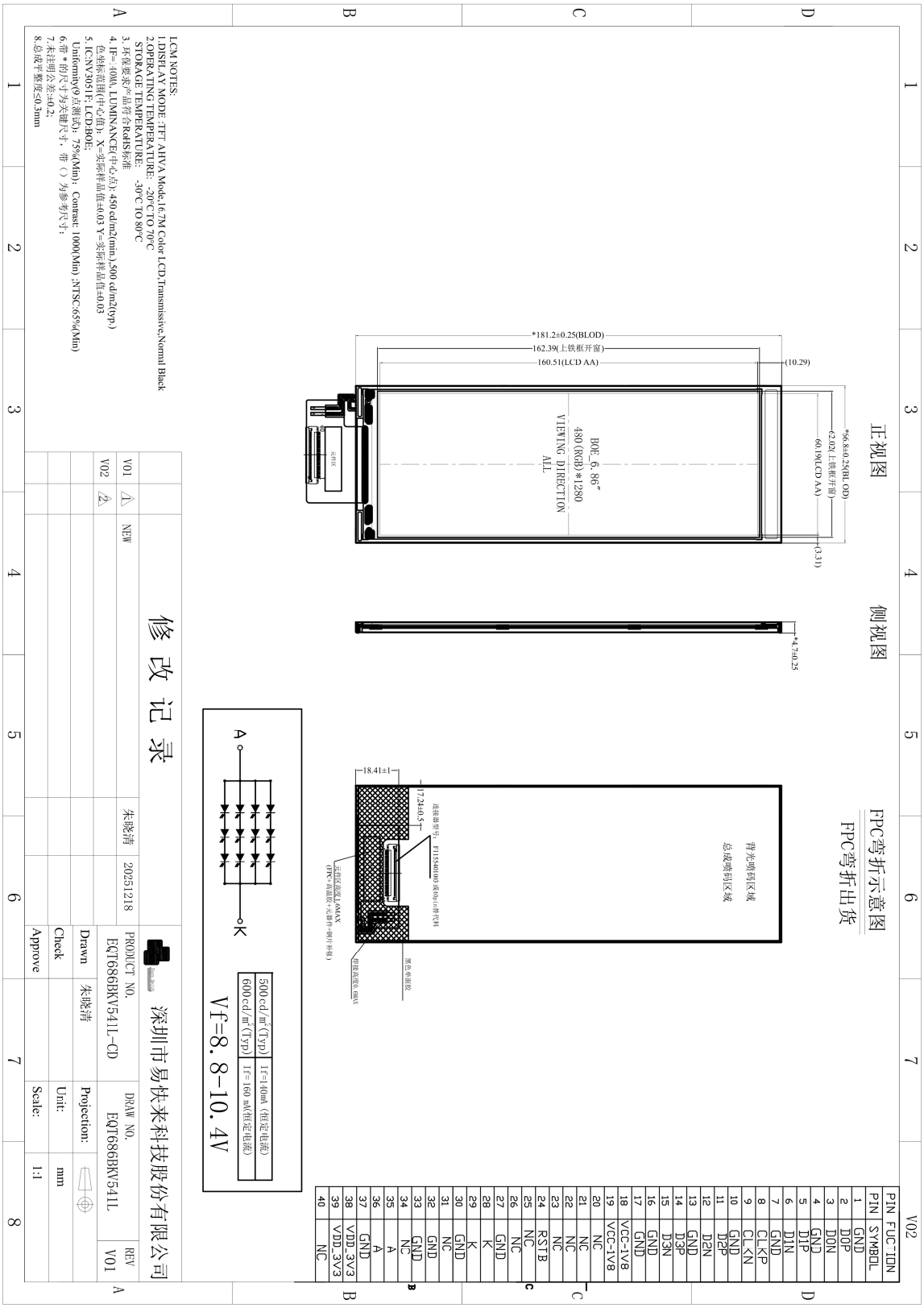


Figure b

FIG.3. The definition of viewing angle



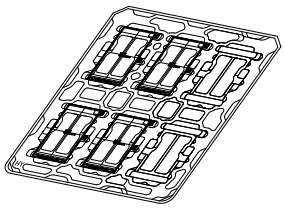
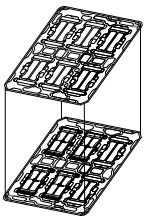
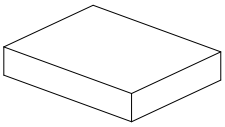
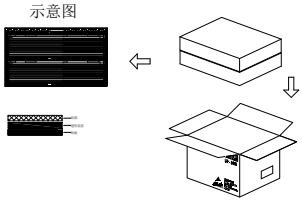
10.LCD Module Outline dimensions （模组外形图 ）



11.Packaging Specification（包装规格）

1.1 Package quantity in one Box : TBD PCS
1.2 Box Size : TBD mm * TBD mm * TBD mm
1.3 1 BOX = TBD CARTON
1.4 1 CARTON = TBD (Full tray) + TBD (dummy / top tray) =TBD tray
1.5 1 TRAY = TBD PCS LCM

注：此为示意图

<table>
<tr>
<td>(1) 模块平放入吸塑盘内，
每盘放6PCS产品
  </td>
<td>(2)吸塑盘交叉叠放
  </td>
<td>(3)十盘加一个空盘共10x6=60pcs
吸塑盘交叉叠放后用胶袋和胶纸打包
叠放次序
B
C
A
C
B
C
A
  </td>
</tr>
<tr>
<td>(4)真空包装
将打包好的产品装进包装袋并抽真空密封，
  </td>
<td>(5) 产品装箱
先在纸箱底下放一个纸板，让后放一小包产品进去，在放一个纸板在上面，最后在放一个纸板在上面，二包叠加装箱
示意图
  </td>
<td>(6) 封箱
外箱标签中须体现供应商名称、EQ料号及包装数量。
 
外箱标签贴于侧面
数量：2x60=120 PCS/箱</td>
</tr>
</table>