PREPARED BY : 制作人 :LYF 日期：2025-12-22	EASYQUICK TECHNOLOGY SPECIFICATION 深圳市易快来科技股份有限公司	SPEC No：（规格型号：） EQT424EEA537G FILE No ：（档案编号 ：） EQ2025122201 ISSUE（日期） 2025-12-22 PAGE（页码） 18
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For **240*1020** TFT LCD Module Model No

EQT424EEA537G

SPEC

Customer side signature（客户方签名）			
签名 / 部门	Acknowled-ge（承认人）	Date（日期）	Remarks（备注）
Structure（结构）			
Electronics（电子）			
Item（项目）			
Quality（品质）			

EASYQUICK TECHNOLOGY

（易快来科技）

1. Application（应用）

This data sheet is to introduce the specification of **EQT424EEA537G** active matrix 16.7M color TFT LCD module.
Main color LCD module is controlled by Driver IC AXS15231B.
If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.
As to basic specification of driver IC refer to the IC specification and handbook.

本规格书是为了介绍 **EQT424EEA537G** 有源矩阵 16.7M 彩色 TFT LCD 模块的规格。
主彩色液晶显示模块由驱动芯片 AXS15231B 控制
本规范未尽事宜如有问题，双方必须认真协商解决。
驱动 IC 的基本规格参照《IC 规格书》和相关《手册》。

2. Construction and Outline （结构与大纲）

Construction: LCD panel, Driver (COG), FPC with electric components, 6 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.
There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.
In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.
So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

结构:液晶面板，驱动或 COG，带电子元件的 FPC, 6 个白光 LED 块，棱镜片，扩散器，导光器和反射器，塑料框架机械固定。
不应有可能影响显示功能的划痕、污迹、芯片、畸变等外部缺陷。
为了实现薄型模块结构，采用双面胶带固定液晶面板。由于这些胶带不能保证永久有效固定面板，LCD 面板在出厂时可能会从模块内移动。
所以在液晶模块组包装和进柜时，请务必将包装结构设计成用海绵等软材料支撑液晶面板的边缘。

3. Mechanical Specification（参数规格）

No.	Item	Contents	Unit
1	Screen size（屏幕尺寸）	4.24 inch	/
2	Display mode（显示模式）	Normally black	/
3	View Angle（视角）	FULL VIEW	/
4	Display format（分辨率）	240×1020	/
5	Outline Dimensions（外形尺寸）	30.32(W)×153.90(H)×2.83(D)	mm
6	Active area（ 显示范围）	24.92(H)×104.67(V)	mm
7	Pixel size(像素）	0.10383 (H) x 0.10262 (V)	mm
8	Interface type（接口类型）	MIPI	/
9	Color Depth（颜色深度）	16.7M	/
10	Module power consumption（模组功耗）	TBD	W
11	Back light type（背光类型）	LED	/
12	Driver IC（驱动 IC）	AXS15231B	/
13	Weight（重量）	TBD	G

Note 1: Not include FPCs & Bezel extrude stucture.

备注 1: 不包括排线和面板构造

4. ABSOLUTE MAXIMUM RATINGS(绝对最高额定值)

Item	Symbol	Min.	Max.	Unit	Note
Power supply voltage(电源输入电压)	VCI	-0.3	+4.0	V	
I/O logic voltage（I/O 逻辑电压）	VDDIO	-0.3	+4.0	V	
Operation temperature（运行温度）	Top	-20	+70	°C	
Storage temperature（储存温度）	Tst	-30	+80	°C	

5. ELECTRICAL CHARACTERISTICS（电气特性）

5.1 TFT DC CHARACTERISTICS(at Ta=25°C)

TFT 直流特性(at Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply input voltage（电源输入电压）	VCI	3.0	3.3	3.6	V	
I/O logic voltage（I/O 逻辑电压）	VDDIO	1.65	1.8	3.6	V	
Input voltage 'H' level（输入电压高水平）	VIH	-	-	-	V	
Input voltage 'L' level（输入电压低水平）	VIL	-	-	-	V	
Power supply current （电源电流）	IVCI	-	TBD	-	mA	
I/O logic voltage current （I/O 逻辑电压电流）	IVDDIO	-	TBD	-	mA	
TFT gate on voltage （TFT门打开电压）/ Input positive voltage(输入正极电压）	VGH/VSP	-	-	-	V	
TFT gate off voltage （TFT门关闭电压）/ Input Negative voltage(输入负极电压）	VGL/VSN	-	-	-	V	
Analog power supply voltage（模拟电源电压）	AVDD	-	-	-	V	
TFT input common mode voltage （TFT输入共模电压）	VCOM	-	-	-	V	Note1

Note1 : The value is just the reference value. The customer can optimize the setting value by the different D-IC

Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..

备注：该值只是参考值，应用于不同的驱动芯片需要优化设定值，VCOM 必须进行调整来优化显示质量，比如串扰、对比度等

5. 2 LED back light（背光灯）

At main panel the back light uses 6 pcs edge light type white LED.
在背光的主面板用 6 颗白色 LED 灯

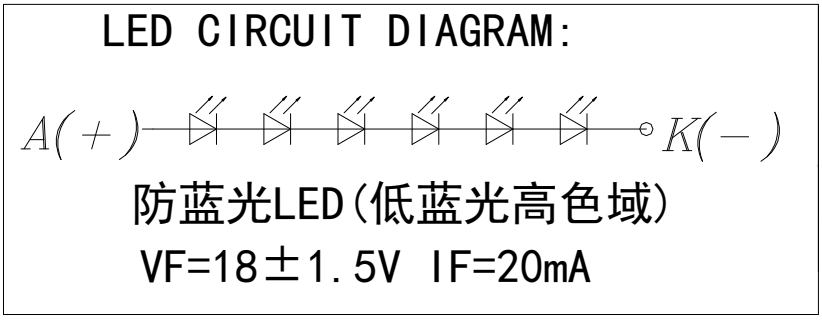


Table 4（表 4）

Parameter（参数）	**Symbol（样品）**	**Min.（最小值）**	**Typ.（标准值）**	**Max.(最大值)**	**Unit（单位）**	**Remark（备注）**
LED Voltage（LED 电压）	VLED	16.5	18	19.5	V	
LED Current（LED 电流）	ILED	-	20	-	mA	
Power Consumption（电功率）	WLED	-	360	-	mW	
Connection Type(Serial/Parallel/Other) 连接类型(串联/并联/其他)		6S1P LEDs				

Note:

*6 pcs of LED

*Please consider Allowable Forward Current on used temperature

*6 颗灯

* 请考虑允许范围内的正向电流的使用温度

Fig.1*Schematics drawing of lighting （绘制照明图 图.1）

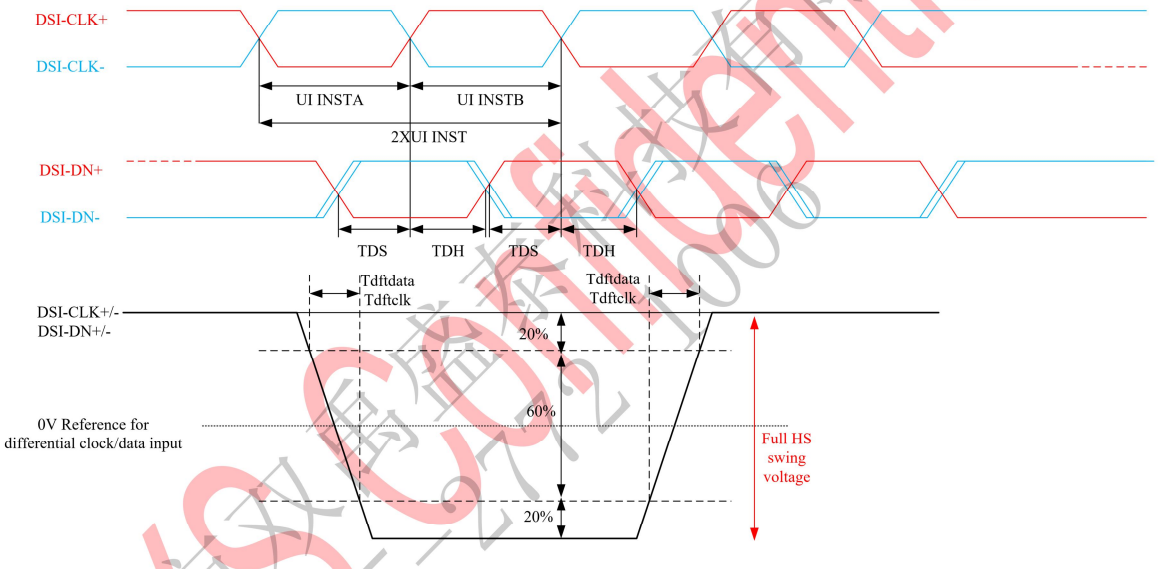
6. Interface signals（接口信号）

TFT Module Interface description（TFT 模块接口描述）

Interface No.	Name	I/O or connect to	Description
1	NC	/	No connection
2	VCC 3.3	P	Power Supply 3.3V
3	IOVCC 3.3	P	Power Supply for I/O System(3.3V)
4	RESET	I	External reset for LCM
5	GND	P	Ground
6	D1P	I	MIPI-DSI data lane positive-end input pin1+
7	D1N	I	MIPI-DSI data lane negative-end input pin1-
8	GND	P	Ground
9	CLKP	I	MIPI-DSI clock lane positive-end input pin+
10	CLKN	I	MIPI-DSI clock lane negative-end input pin-
11	GND	P	Ground
12	D0P	I/O	MIPI-DSI data lane positive-end input pin 0+
13	D0N	I/O	MIPI-DSI data lane negative-end input pin 0-
14	GND	P	Ground
15	TE	O	Tearing effect output pin
16	LEDA	P	Power for LED backlight(Anode)
17	NC	/	No connection
18	LEDK	P	Power for LED backlight(Cathode)
19	ID2	O	LCD ID
20	TP_VCC	/	No connection
21	TP_RESET	I	TP Reset, low active
22	TP_INT	I/O	TP Interrupt pin
23	TP_SDA	I/O	I2C interface data pin
24	TP-SCL	I/O	I2C interface clock pin
25	GND	P	Ground
33	GND	P	Ground

7. AC CHARACTERISTICS（交流特性）

5.4.7.1. High speed mode



Parameter	Symbol	Parameter	Specification			Unit	Description
			MIN	TYP	MAX		
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4		25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2		12.5	ns	$UI=UI_{INSTA}=UI_{INSTB}$
DSI-D0+/-	T_{DS}	Data to clock setup time	0.15	-		UI	
DSI-D0+/-	T_{DH}	Data to clock hold time	0.15	-		UI	

Figure: AC characteristics for MIPI-DSI High speed mode

5.4.7.2. Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP -11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP -11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2XT_{LPXD}$	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to driver LP-00 by display module	$5XT_{LPXD}$	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to driver LP-00 after turnaround request - MPU	$4XT_{LPXD}$	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	

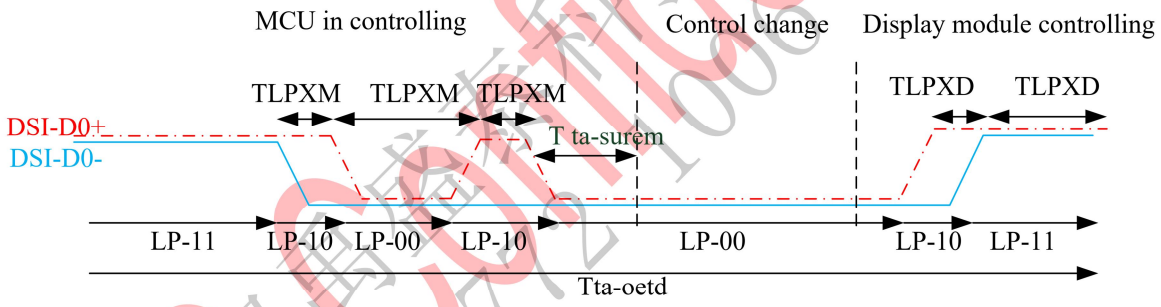


Figure: BTA from the MCU to the Display Module

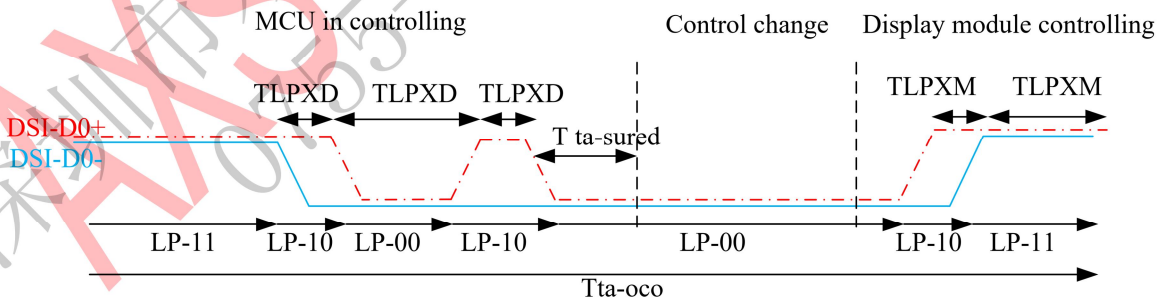


Figure: BTA from the Display Module to the MCU

5.4.7.3. Bursts

Parameter	Symbol	Parameter	Specification	Unit

			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to driver LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to driver HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lanereceiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to driver flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ Period to start of LP-11 state	-	-	105ns +12UI	ns

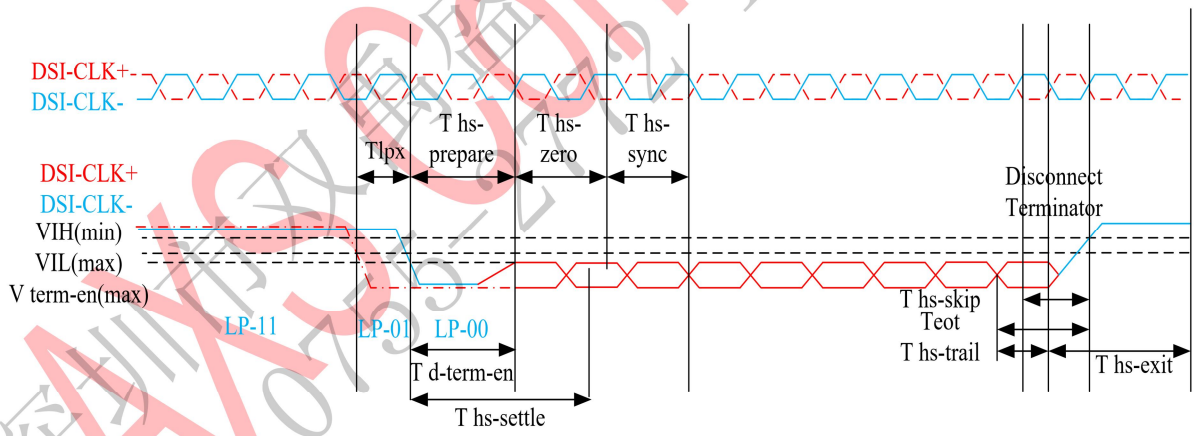


Figure: High Speed Data Transmission Bursts

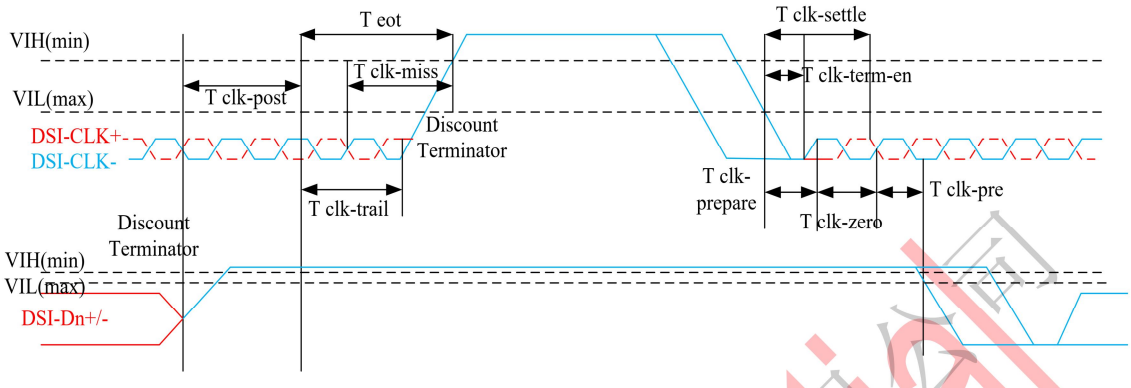


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lanehas transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be drivern prior to any associated Data Lanebeginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to driver LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lanereceiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$+ time for lead HS-0 drivcr pcriod bcforc starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to driver HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ periodto start of LP-11 state	-	-	105ns + 12UI	ns

5.4.7.4. LP-11 between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-

11) when
different combinations, what are listed below, are possible:
1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode
The Low Power Mode is also including 2 different functions:
1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-11) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100ns	-	100ns	-	100ns	-
HSDT	60ns+52UI	-	60ns+52UI	-	60ns+52UI	-
BTA	100ns	-	100ns	-	100ns	-

8. POWER SEQUENCE（电源时序）

6.1. Normal Power On/Off Sequence

VDDI and VCI can be applied in any order. VDDIand VCI can be powered down in any order. In a MCU system, VDDI is typically generated from VCI by a DC-DC or LDO converter. So generally speaking, VDDI is powered up after the VCI.

During power off, if LCD is in the Sleep Out mode, VDDI and VCI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

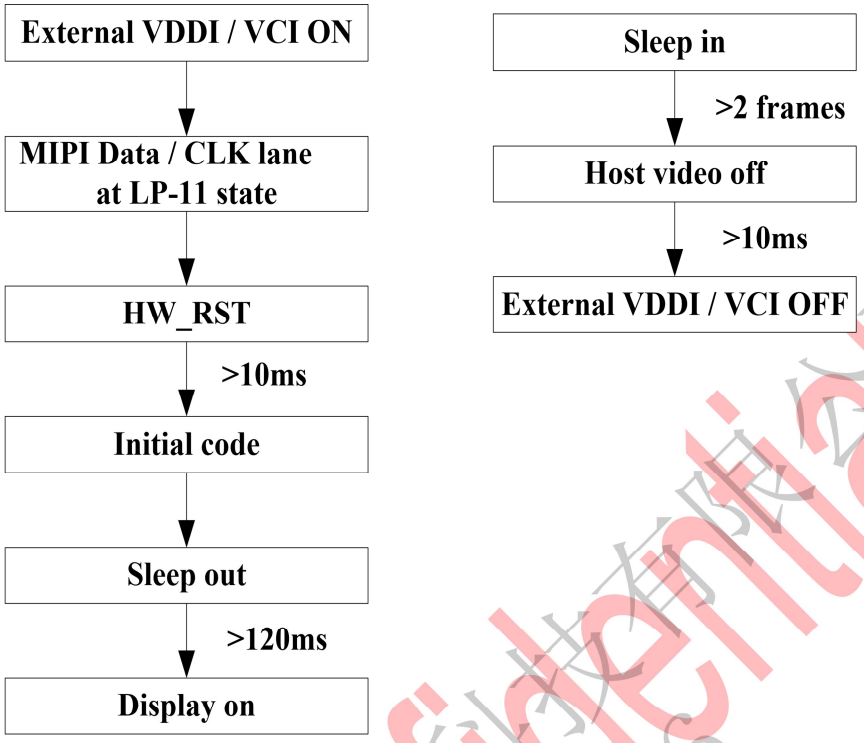
Note 1: There will be no damage to the display module if the power sequences are not met.

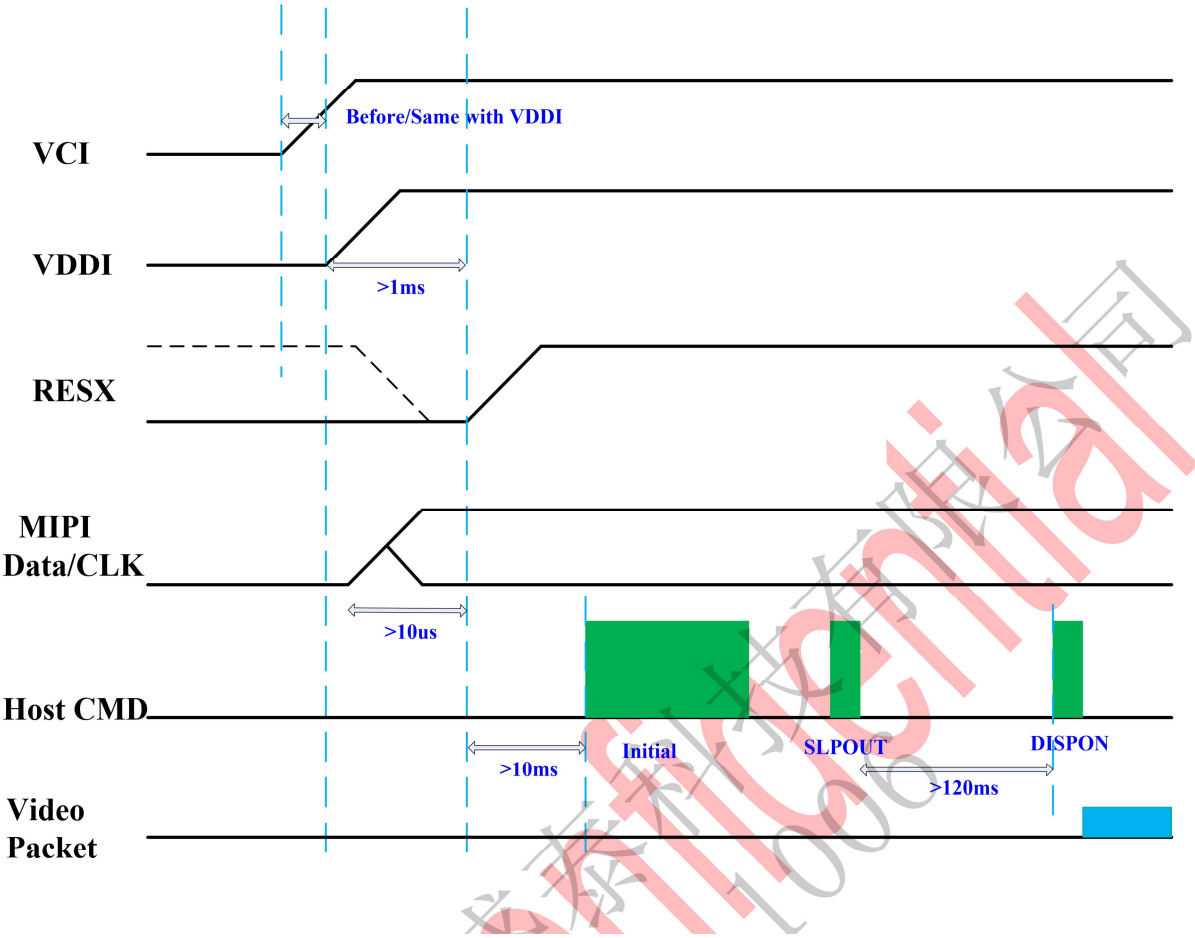
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

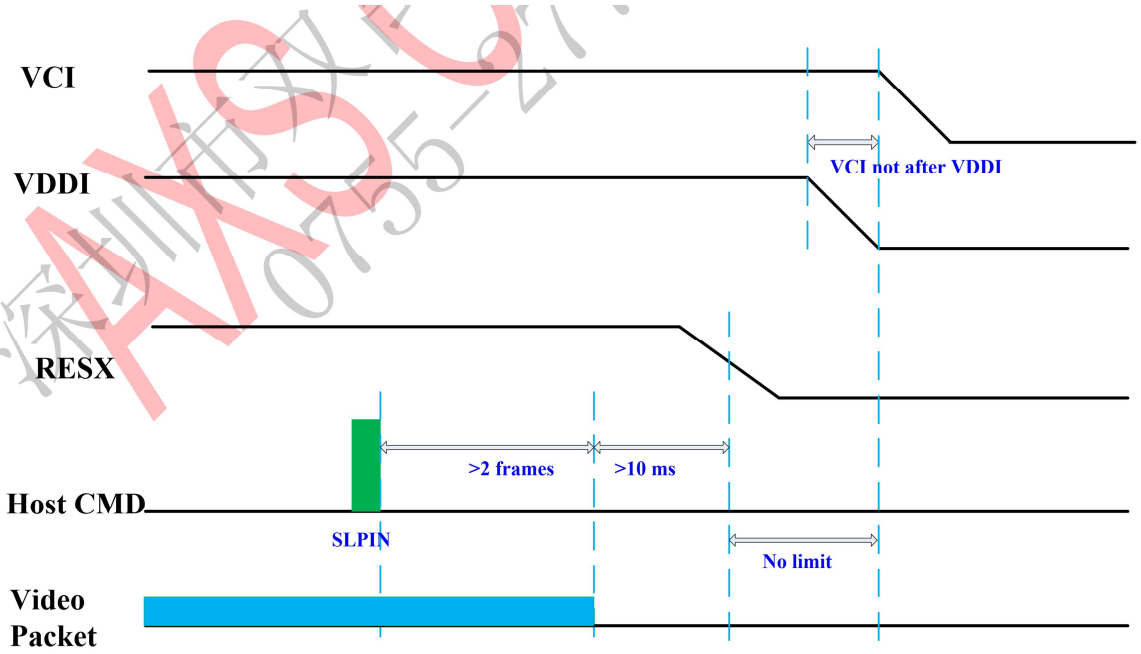
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command.

Also, between receiving Sleep In command and Power Off Sequence. If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise, function is not guaranteed.

The power on/off sequence is illustrated below:


External VDDI / VCI ON
MIPI Data / CLK lane at LP-11 state
HW_RST
>10ms
Initial code
Sleep out
>120ms
Display on
Sleep in
>2 frames
Host video off
>10ms
External VDDI / VCI OFF

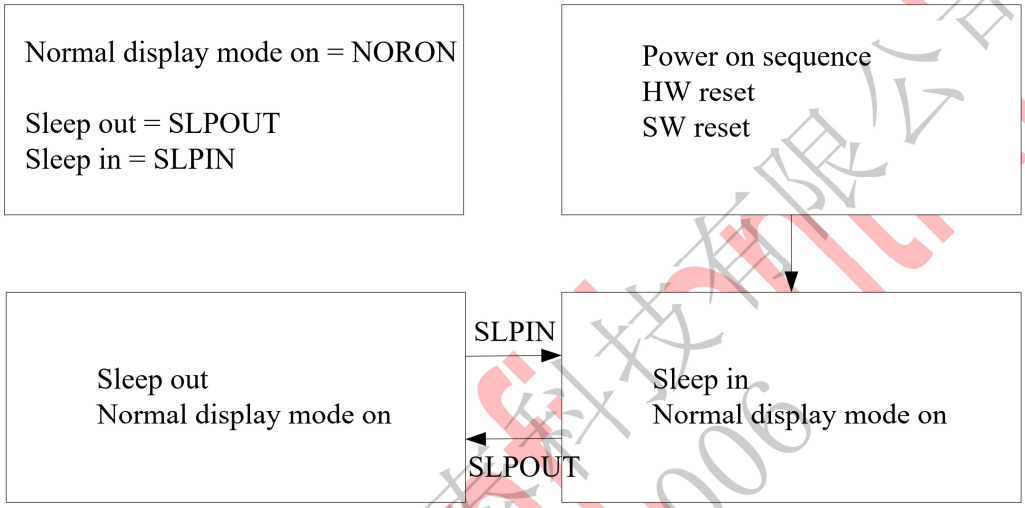

VCI
VDDI
RESX
MIPI Data/CLK
Host CMD
Video Packet
Before/Same with VDDI
>1ms
>10us
>10ms
Initial
SLPOUT
>120ms
DISPON



6.2. Abnormal Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damage for the display module or the display module will not cause any damage to the host or lines of the interface. At an uncontrolled power off event, the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

6.3. Power flow chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.

9. Optical Characteristics（光学特征）

Item 项目		Symbol（样品）	Condition（条件）	Min.（最小值）	Typ.（标准值）	Max.（最大值）	Unit（单位）	Remark（备注）
Response time（响应时间）	Rise（上升）+Fall（下降）	Tr +Tf	θ=0°	-	35	45	ms	Note 1 FIG.1
Luminance（亮度）		Br	θ=0°	300	350	-	Cd/m^2	Note 3 FIG.2
Luminance uniformity（亮度均匀性）		YU	θ=0°	80	85	-	%	Note 4 FIG.2
Contrast ratio（对比度）		CR	θ=0°	700	-	-	-	Note 2 FIG.2
Viewing angle(with Polarizer)（视角）	Top（顶部）		CR≥10	-	80	-	degree	Note 6 FIG.3
	Bottom（底部）			-	80	-		
	Left（左边）			-	80	-		
	Right（右边）			-	80	-		
chromaticity coordinates（色坐标）	White（白色）	X	CIE	0.27	0.30	0.33	-	Note 5 FIG.2 CIE1931
		Y		0.28	0.31	0.34		
NTSC（色彩饱和度）			-	75	80	-	%	Note 5 FIG.2

Note1. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state.Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%.

And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

Note2.Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula.

For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

Measured at the center area of the LCD

Note3.Definition of surface luminance

Surface luminance is the luminance with all pixels displaying white.

For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note4.Definition of luminance uniformity

The luminance uniformity in surface luminance is det-ermined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$Yu = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.

For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON's BM-5or BM-7 photo detector or compatible.

FIG.1. The definition of response Time

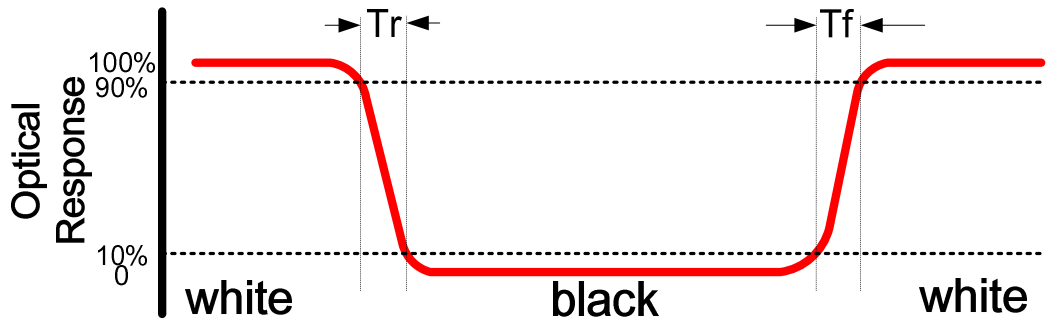


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

H,V : Active area

Light spot size ∅=1.5mm (BM-7)50cm distance or compatible distance from the LCM surface to detector lens.

Test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-7 or compatible ,see Figure b.

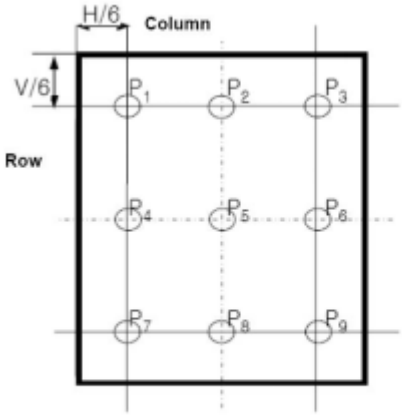


Figure a

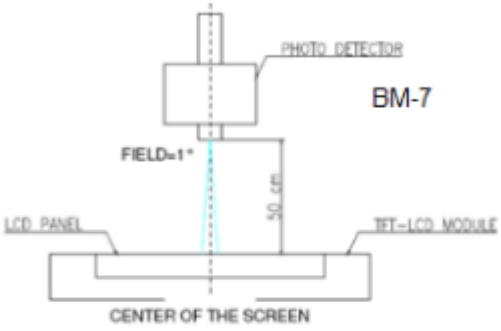
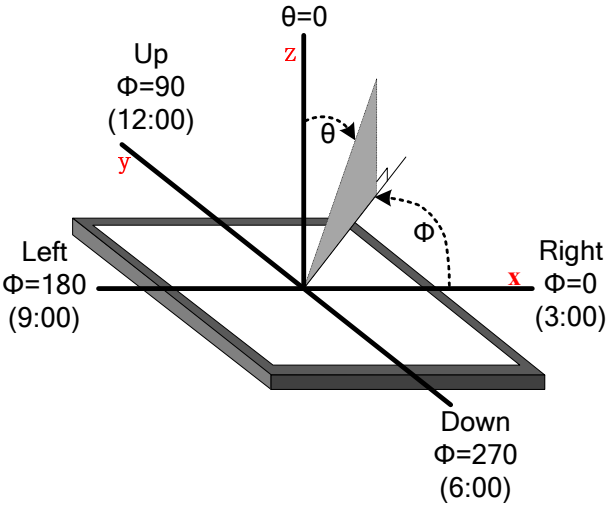
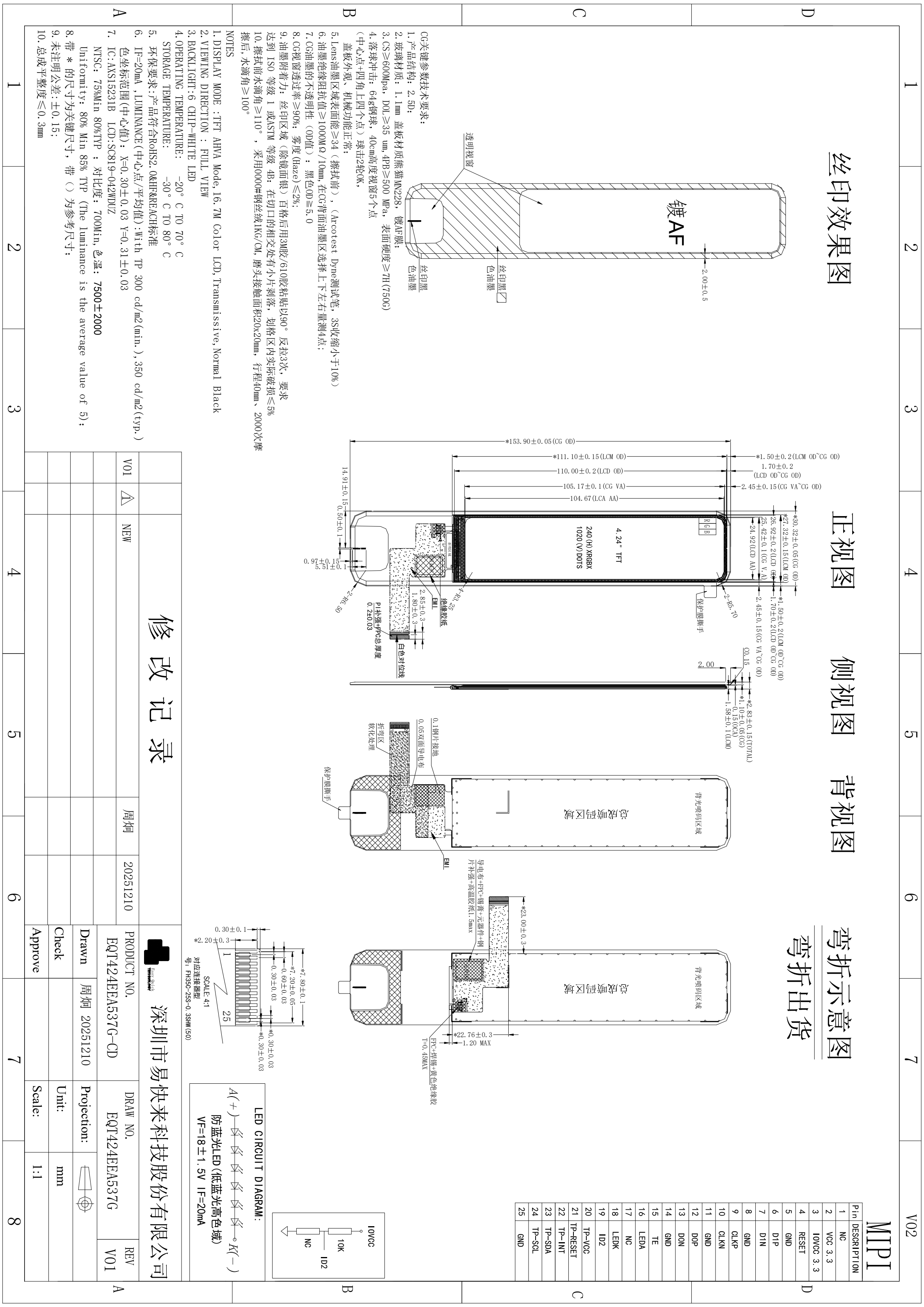


Figure b

FIG.3. The definition of viewing angle



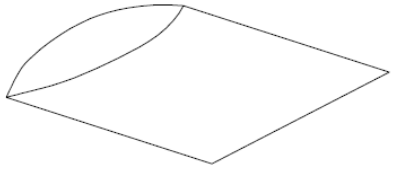
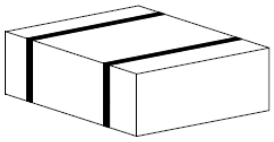
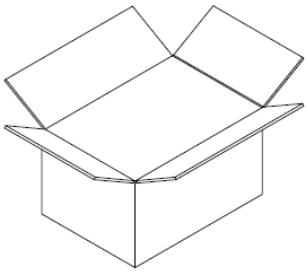
10.LCD Module Outline dimensions （模组外形图 ）



11.Packaging Specification（包装规格）

1.1 Package quantity in one Box : TBD PCS
1.2 Box Size : TBD mm * TBD mm * TBD mm
1.3 1 BOX = TBDCARTON
1.4 1 CARTON = TBD (Full tray) +TBD (dummy / top tray) =TBD tray
1.5 1 TRAY =TBD PCS LCM

注：此为示意图

1.将产品放入吸塑盘内，每盘放 X PCS产品 	2.将吸塑盘叠放在一起，N+1(空盘)，两端用胶带固定 	3.将打包好的吸塑放入到包装袋中 
4.将包装袋固定好为一小包，根据客户要求选择是否贴标签 	5.产品装箱，先在纸箱底部放一层纸板，接着放入1包产品，在包装好的产品上再放一层纸板，然后再放入一包打包好的产品，最后盖上一张纸板后封箱 	6.封箱后在外箱侧面贴外箱标签