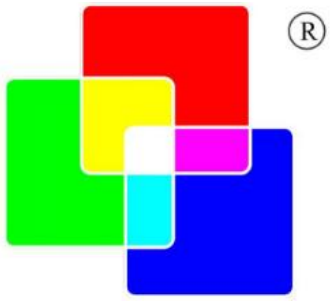
PREPARED BY : 制作人:CLM 日期：2025-12-05	 **EASYQUICK TECHNOLOGY** SPECIFICATION 深圳市易快来科技股份有限公司	SPEC No：（规格型号：） **EQT350BYJ529Z**
R&D APPROVED BY: 审核:GJM 日期：2025-12-05		FILE No ：（档案编号 ：） **EQ2025120501** ISSUE（日期） **2025-12-05** PAGE（页码） **19**
QC APPROVED BY: 确认：WSL 日期：2025-12-05		APPLICABLE DIVISION （适用范围） ■LCD DIVISION ■液晶模组

For **640*480**TFT LCD Module Model No

EQT350BYJ529Z
SPEC

Customer side signature（客户方签名）			
签名 / 部门	Acknowled-ge（承认人）	Date（日期）	Remarks（备注）
Structure（结构）			
Electronics（电子）			
Item（项目）			
Quality（品质）			

EASYQUICK TECHNOLOGY

（易快来科技）

1. Application（应用）

This data sheet is to introduce the specification of **EQT350BYJ529Z** active matrix **16.7M** color TFT LCD module.
Main color LCD module is controlled by Driver IC **JD9365DA**.
If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.
As to basic specification of driver IC refer to the IC specification and handbook.

本规格书是为了介绍 **EQT350BYJ529Z** 有源矩阵 **16.7M** 彩色 TFT LCD 模块的规格。
主彩色液晶显示模块由驱动芯片 **JD9365DA** 控制。
本规范未尽事宜如有问题，双方必须认真协商解决。
驱动 IC 的基本规格参照《IC 规格书》和相关《手册》

2. Construction and Outline （结构与大纲）

Construction: LCD panel, Driver (COG), FPC with electric components, 12 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.
There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.
In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.
So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

结构:液晶面板，驱动或 COG，带电子元件的 FPC, 12 个白光 LED 块，棱镜片，扩散器，导光器和反射器，塑料框架机械固定。
不应有可能影响显示功能的划痕、污迹、芯片、畸变等外部缺陷。
为了实现薄型模块结构，采用双面胶带固定液晶面板。由于这些胶带不能保证永久有效固定面板，LCD 面板在出厂时可能会从模块内移动。
所以在液晶模块组包装和进柜时，请务必将包装结构设计成用海绵等软材料支撑液晶面板的边缘。

3. Mechanical Specification（参数规格）

No.	Item	Contents	Unit
1	Screen size（屏幕尺寸）	3.5	inch
2	Display mode（显示模式）	Normally black	/
3	View Angle（视角）	FULL VIEW	/
4	Display format（分辨率）	640×RGB×480	/
5	Outline Dimensions（外形尺寸）	82.93(W)×65.37(H)×4.59(D)	mm
6	Active area（ 显示范围）	70.08(H)×52.56(V)	mm
7	Cover Glass View area（盖板 VA）	69.41（H）×51.86（V）	mm
8	Pixel size(像素）	0.1095 (H) x 0.1095 (V)	mm
9	Interface type（接口类型）	MIPI	/
10	Color Depth（颜色深度）	16.7M	/
11	Module power consumption（模组功耗）	TBD	W
12	Back light type（背光类型）	LED	/
13	Driver IC（驱动 IC）	JD9365DA(TFT)	/
14	Weight（重量）	TBD	G

Note 1: Not include FPCs & Bezel extrude stucture.

备注 1: 不包括排线和面板构造

4. ABSOLUTE MAXIMUM RATINGS(绝对最高额定值)

Item	Symbol	Min.	Max.	Unit	Note
I/O logic voltage（I/O 逻辑电压）	VDDI	-0.3	+3.6	V	
Supply voltage（供电电压）	AVDD	-0.3	+6.6	V	
Supply voltage（供电电压）	AVEE	0	+6.6	V	
Operation temperature（运行温度）	Top	-20	+70	°C	
Storage temperature（储存温度）	Tst	-30	+80	°C	

5. ELECTRICAL CHARACTERISTICS（电气特性）

5.1 TFT DC CHARACTERISTICS(at Ta=25°C)

TFT 直流特性(at Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply input voltage（电源输入电压）	VDD	-	-	-	V	
I/O logic voltage（I/O 逻辑电压）	VDDI	1.65	-	3.6	V	
Input voltage 'H' level（输入电压高水平）	VIH	0.7VDDI	-	VDDI	V	
Input voltage 'L' level（输入电压低水平）	VIL	0	-	0.3VDDI	V	
Power supply current （电源电流）	IVDD	-	TBD	-	mA	
I/O logic voltage current （I/O 逻辑电压电流）	IVDDIO	-	TBD	-	mA	
TFT gate on voltage （TFT门打开电压）/ Input positive voltage(输入正极电压）	VSP	5	5.5	6.3	V	
TFT gate off voltage （TFT门关闭电压）/ Input Negative voltage(输入负极电压）	VSN	-6.3	-5.5	-5	V	
Analog power supply voltage（模拟电源电压）	AVDD	-	-	-	V	
TFT input common mode voltage （TFT输入共模电压）	VCOM	-	-	-	V	Note1

Note1 : The value is just the reference value. The customer can optimize the setting value by the different D-IC

Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..

备注：该值只是参考值，应用于不同的驱动芯片需要优化设定值，VCOM 必须进行调整来优化显示质量，比如串扰、对比度等

5. 2 LED back light（背光灯）

At main panel the back light uses 12 pcs edge light type white LED.
在背光的主面板用 12 颗白色 LED 灯

Table 4（表 4）

Parameter（参数）	Symbol（样品）	Min.（最小值）	Typ.（标准值）	Max.（最大值）	Unit（单位）	Remark（备注）
LED Voltage（LED 电压）	VLED	16.2	18	19.8	V	
LED Current（LED 电流）	ILED	-	40	-	mA	
Power Consumption（电功率）	WLED	-	720	-	mW	
Connection Type(Serial/Parallel/Other) 连接类型(串联/并联/其他)		6S2P LEDs				

Note:
*12 pcs of LED
*Please consider Allowable Forward Current on used temperature
*12 颗灯
* 请考虑允许范围内的正向电流的使用温度

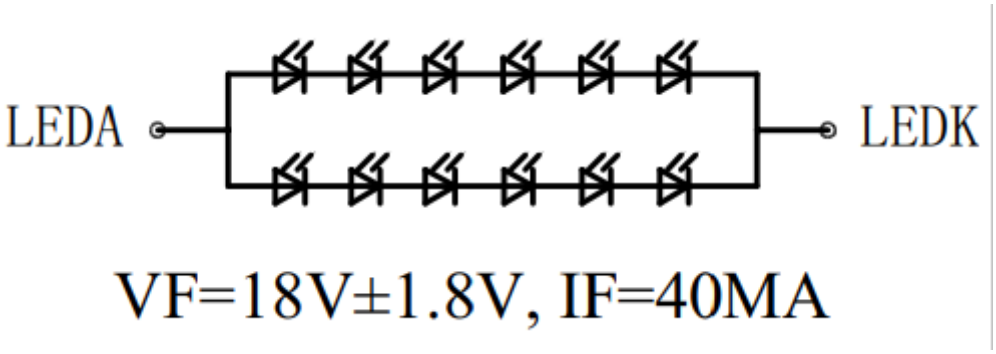


Fig.1*Schematics drawing of lighting （绘制照明图 图.1）

6. Interface signals（接口信号）

TFT Module Interface description（TFT 模块接口描述）

Interface No.	Name	I/O or connect to	Description
1-2	GND	P	Ground
3-5	NC	/	NC
6-7	GND	P	Ground
8-9	AVDD	P	Analog power supply (AVDD)
10-11	AVEE	P	Analog power supply (AVEE)
12-13	GND	P	Ground
14	VIO(1.8V)	P	Power Supply
15	GND	P	Ground
16	TE	O	Tearing effect output pin
17	LCM RESET	I	LCD reset pin
18	ID	O	ID for LCD
19	GND	P	Ground
20	TDP3	I	MIPI-DSI data Lane 3 positive-end input pin
21	TDN3	I	MIPI-DSI data Lane 3 negative-end input pin
22	GND	P	Ground
23	TDP2	I	MIPI-DSI data Lane 2 positive-end input pin
24	TDN2	I	MIPI-DSI data Lane 2 negative-end input pin
25	GND	P	Ground
26	TCP	I	MIPI-DSI clock Lane positive-end input pin
27	TCN	I	MIPI-DSI clock Lane negative-end input pin
28	GND	P	Ground
29	TDP1	I	MIPI-DSI data Lane 1 positive-end input pin
30	TDN1	I	MIPI-DSI data Lane 1 negative-end input pin
31	GND	P	Ground
32	TDP0	I	MIPI-DSI data Lane 0 positive-end input pin
33	TDN0	I	MIPI-DSI data Lane 0 negative-end input pin
34-35	GND	P	Ground
36	LEDA	P	Power for LED backlight(Anode)
37-38	LEDK	P	Power for LED backlight(Cathode)
39	GND	P	Ground

7. AC CHARACTERISTICS（交流特性）

7.1 MIPI Interface Characteristics:

High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 13.5.

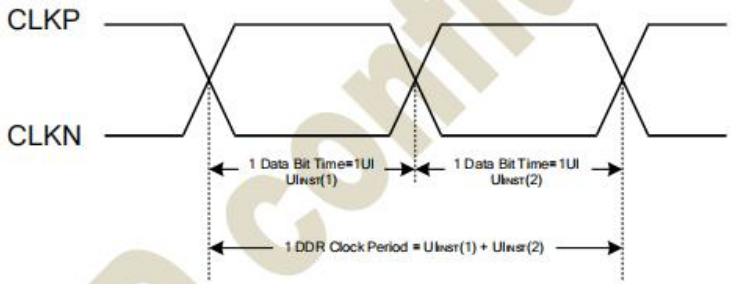


Figure 11.5: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1), (2), (3), (4), (5), (6)

Note: (1) This value corresponds to a minimum 80 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 850bps of 1 data lane 24-bit data format/ 630Mbps of 1 data lane 18-bit data format/ 560Mbps of 1 data lane 16-bit data format.
(4) Maximum total bit rate is 1.7Gbps of 2 data lanes 24-bit data format/ 1.27Gbps of 2 data lane 18-bit data format/ 1.13Gbps of 2 data lane 16-bit data format.
(5) Maximum total bit rate is 2Gbps of 3 data lanes 24-bit data format/ 1.5Gbps of 3 data lane 18-bit data format/ 1.33Gbps of 3 data lane 16-bit data format.
(6) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format/ 1.5Gbps of 4 data lane 18-bit data format/ 1.33Gbps of 4 data lane 16-bit data format.

Table 11.11: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.13. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

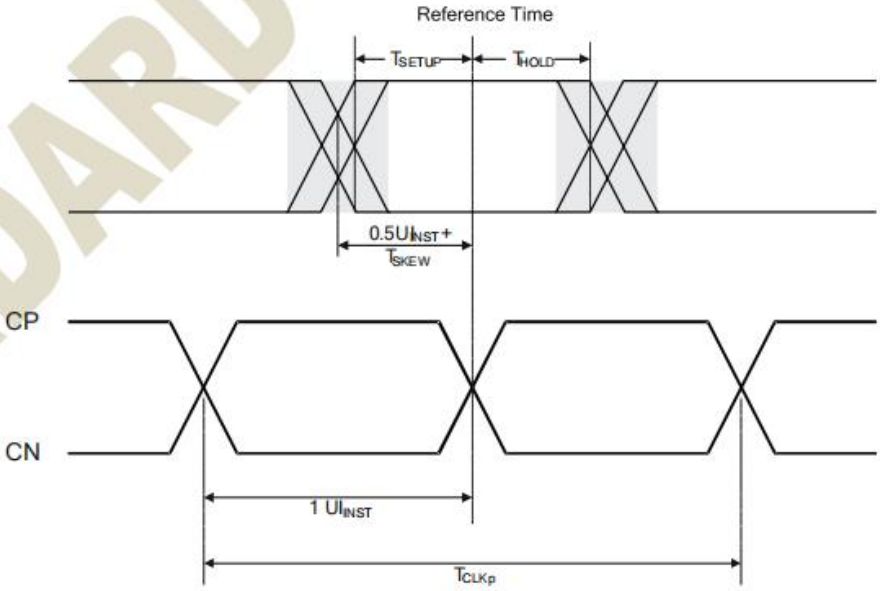


Figure 11.6: Data to Clock Timing Definitions

7.2 Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 13.12. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 13.12 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm 0.2*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UIINST.

Table 11.12: Data to Clock Timing Specifications

7.3Burst Mode Data Transmission

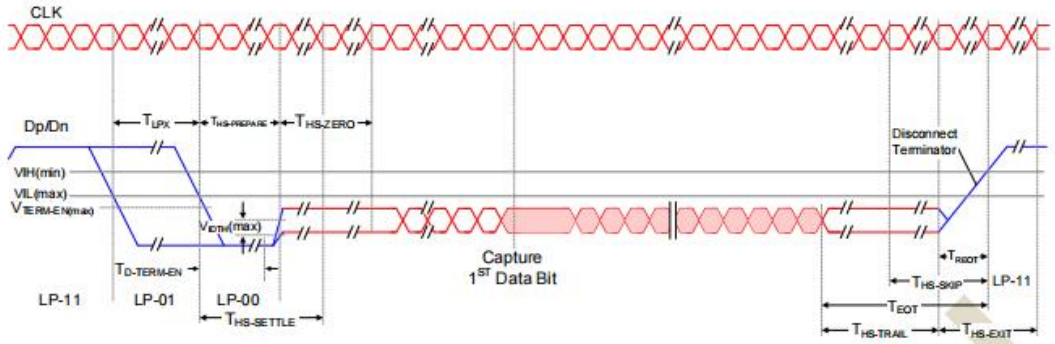


Figure 11.7: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 + n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

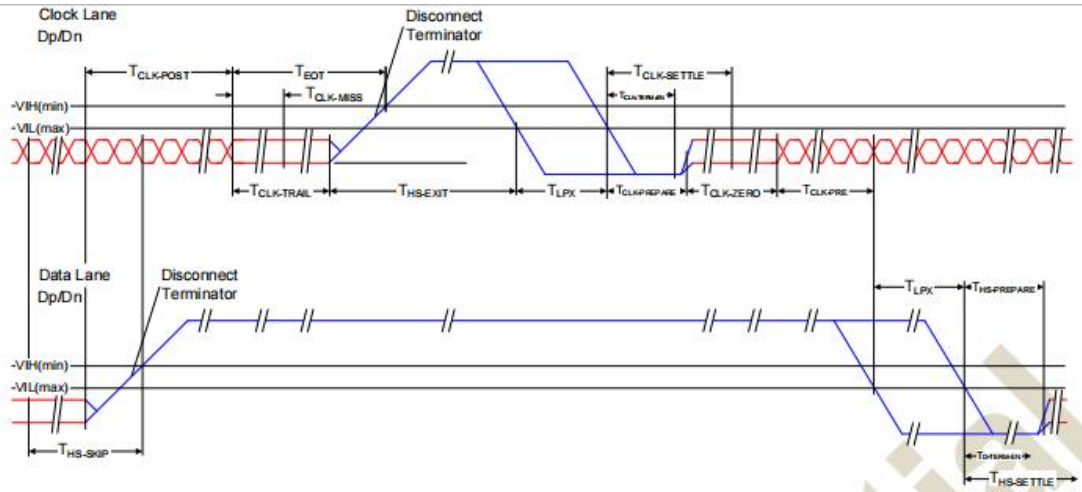


Figure 11.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

7.4 Reset TIming

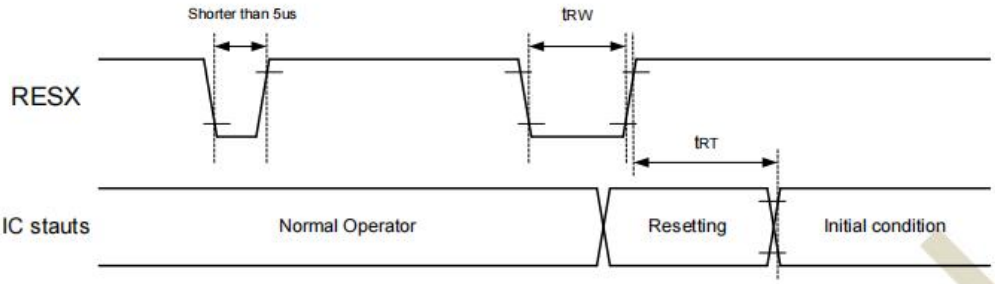


Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	10	-	μs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

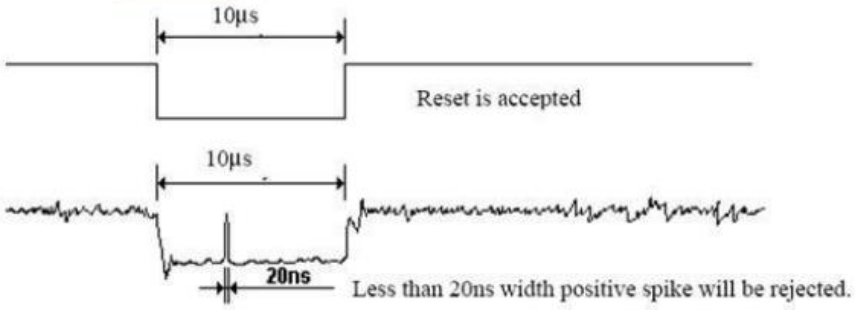
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

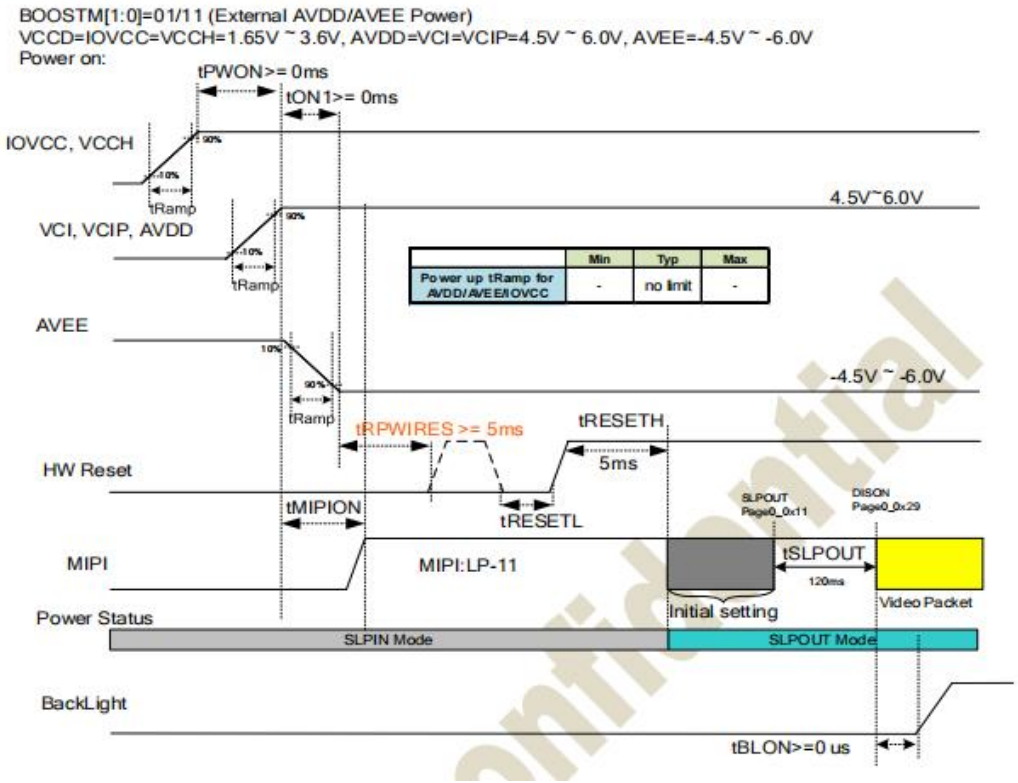
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

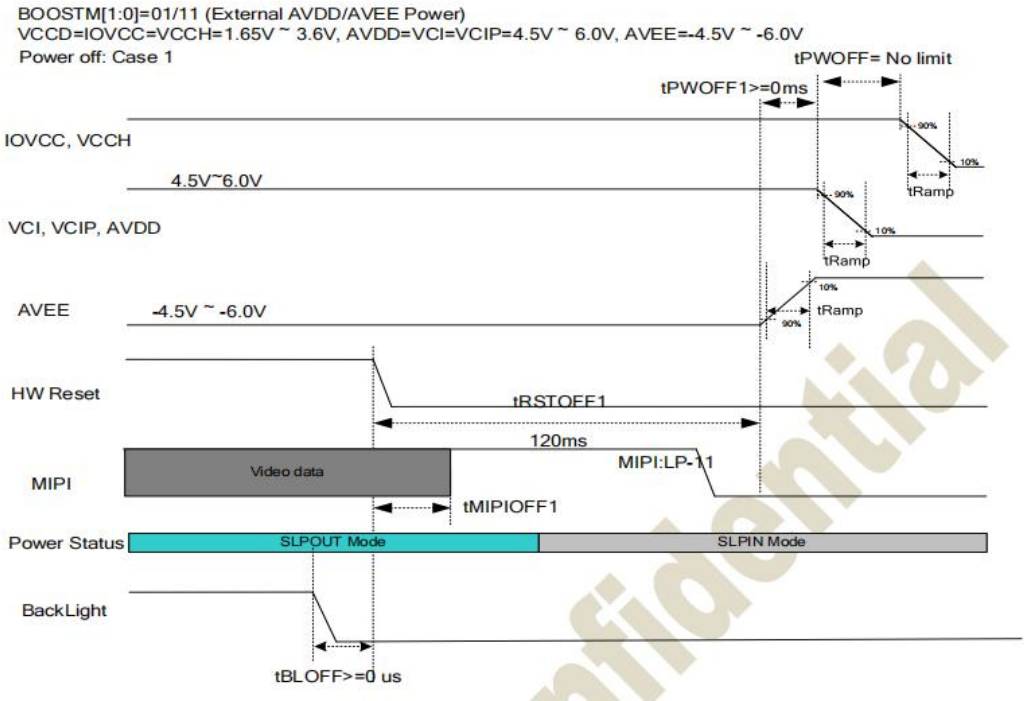
Table 11.3: Reset timings

8. POWER SEQUENCE（电源时序）

Power-on sequence



Power-off sequence



9. Optical Characteristics（光学特征）

Item 项目		Symbol（样品）	Condition（条件）	Min.（最小值）	Typ.（标准值）	Max.（最大值）	Unit（单位）	Remark（备注）
Response time（响应时间）	Rise（上升）+Fall（下降）	Tr +Tf	θ=0°	-	25	35	ms	Note 1 FIG.1
Luminance（亮度）		Br	θ=0°	350	400	-	Cd/m^2	Note 3 FIG.2
Luminance uniformity（亮度均匀性）		YU	θ=0°	80	-	-	%	Note 4 FIG.2
Contrast ratio（对比度）		CR	θ=0°	900	1200	-	-	Note 2 FIG.2
Viewing angle(with Polarizer)（视角）	Top（顶部）		CR≥10	80	85	-	degree	Note 6 FIG.3
	Bottom（底部）			80	85	-		
	Left（左边）			80	85	-		
	Right（右边）			80	85	-		
White Chromaticity（白色色度）		X	CIE	0.275	0.305	0.335	-	Note 5 FIG.2 CIE1931
		Y		0.3	0.33	0.36	-	
NTSC（色彩饱和度）			-	55	60	-	%	Note 5 FIG.2

Note1. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state.Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%.

And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

Note2.Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula.

For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

Measured at the center area of the LCD

Note3.Definition of surface luminance

Surface luminance is the luminance with all pixels displaying white.

For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note4.Definition of luminance uniformity

The luminance uniformity in surface luminance is det-ermined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$Yu = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.

For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON's BM-5or BM-7 photo detector or compatible.

FIG.1. The definition of response Time

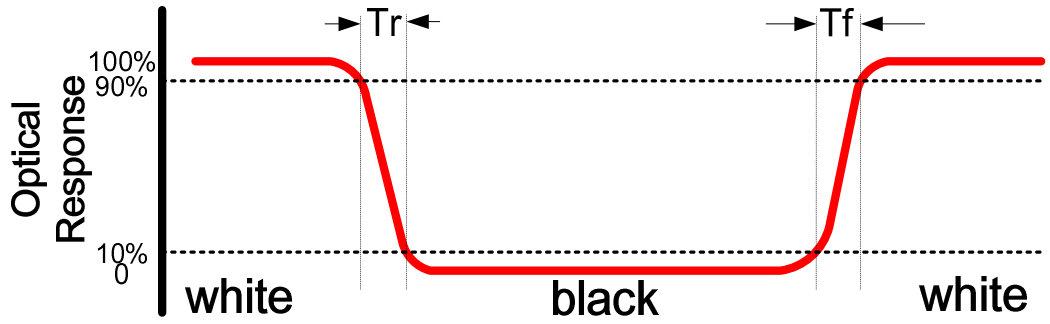


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

H,V : Active area

Light spot size ∅=1.5mm (BM-7)50cm distance or compatible distance from the LCM surface to detector lens.

Test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-7 or compatible ,see Figure b.

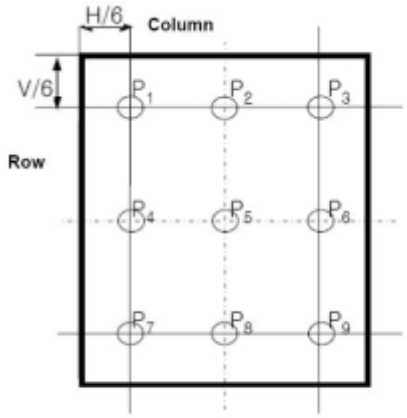


Figure a

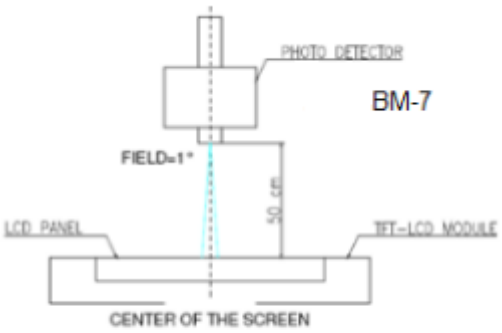
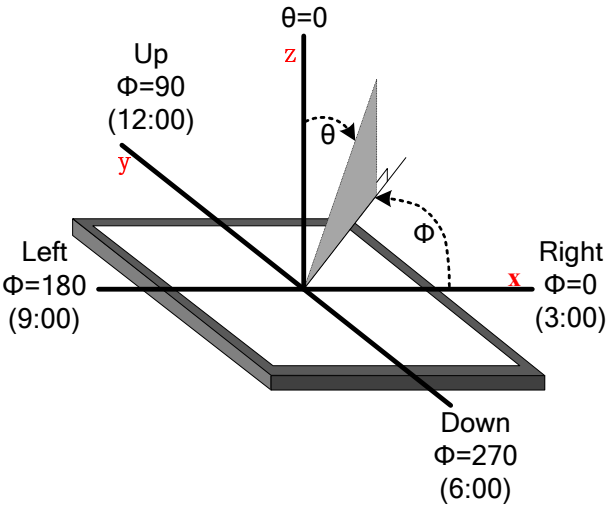
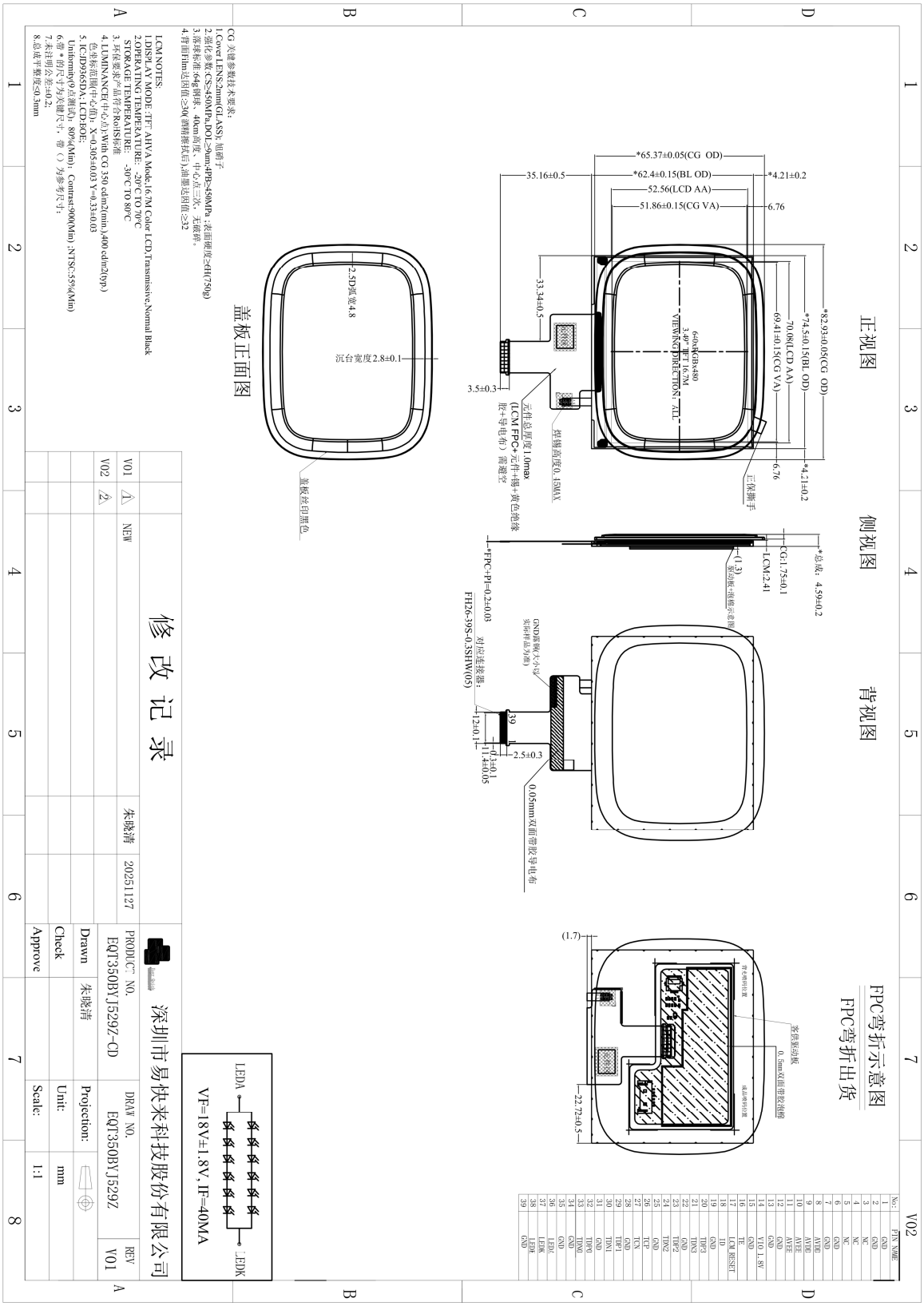


Figure b

FIG.3. The definition of viewing angle

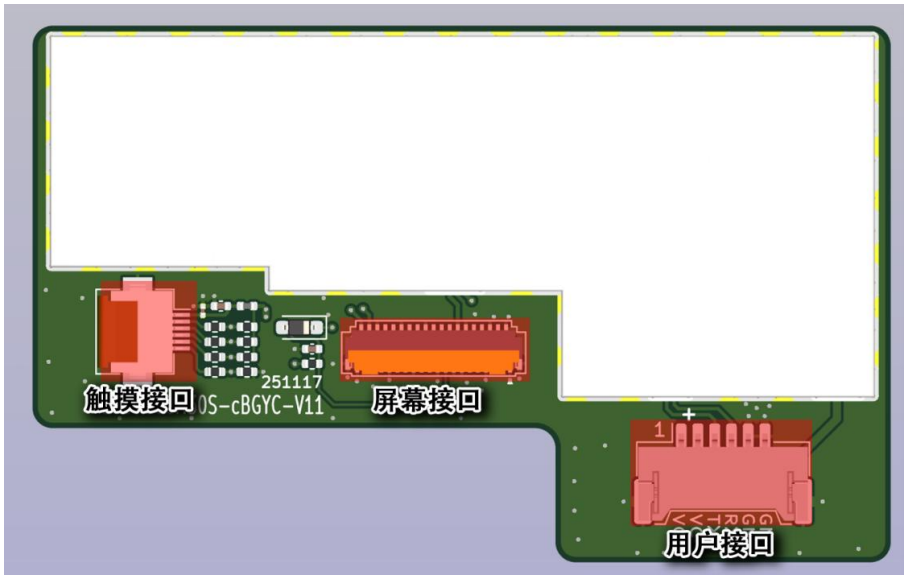


10.LCD Module Outline dimensions （模组外形图 ）



11.Packaging Specification（PCBA）

1.1PCBA 示意图



1.2 接口描述：

接口描述	接口封装	备注
调试串口	MX1.25-7P	默认不贴装
用户接口	MX1.25-ST-6P	超薄 MX1.25
下载 USB	接口 PinHeader 2.54mm 1x3P	默认不贴装
触摸接口	FPC-0.5MM-6P	
屏幕接口	FPC-0.5MM-39P	

1.3 用户接口定义

接口序号	接口定义	电压范围	备注
1	+BATT	3.5V~6V	接电池电压或 5V 电源
2	+BATT	3.5V~6V	接电池电压或 5V 电源
3	TXD	3.3V TTL	串口信号输出
4	RXD	3.3V TTL	串口信号输入
5	GND	0V	接地
6	GND	0V	接地

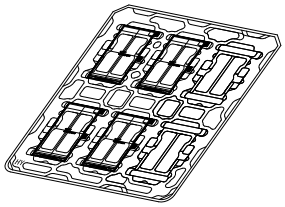
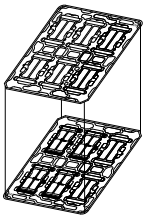
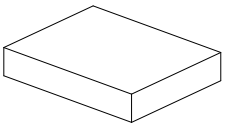
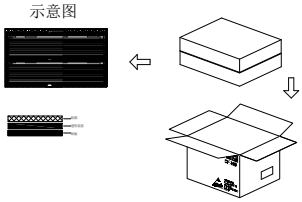
1.4 调式串口定义

接口序号	接口定义	电压范围	备注
1	+5V	5V	
2	NC	NC	
3	TXD	3.3V TTL	串口信号输出
4	RXD	3.3V TTL	串口信号输入
5	RESET	0-3.3V	芯片使能
6	BOOT (TXD)	0-3.3V	BOOT 与 TXD 复用
7	GND	0V	接地

12. Packaging Specification（包装规格）

1.1 Package quantity in one Box : TBD PCS
1.2 Box Size : TBD mm * TBD mm * TBD mm
1.3 1 BOX = TBD CARTON
1.4 1 CARTON = TBD(Full tray) + TBD (dummy / top tray) =TBD tray
1.5 1 TRAY = TBD PCS LCM

注：此为示意图

<table>
<tr>
<td>(1) 模块平放入吸塑盘内，
每盘放6PCS产品
  </td>
<td>(2)吸塑盘交叉叠放
  </td>
<td>(3)十盘加一个空盘共10x6=60pcs
吸塑盘交叉叠放后用胶袋和胶纸打包
叠放次序
B
C
A
C
B
C
A
  </td>
</tr>
<tr>
<td>(4)真空包装
将打包好的产品装进包装袋并抽真空密封，
  </td>
<td>(5) 产品装箱
先在纸箱底下放一个纸板,让后放一小包产品进去，在放一个纸板在上面，最后在放一个纸板在上面，二包叠加装箱
示意图
  </td>
<td>(6) 封箱
外箱标签中须体现供应商名称、EQ料号及包装数量。
 
外箱标签贴于侧面
数量：2x60=120 PCS/箱</td>
</tr>
</table>