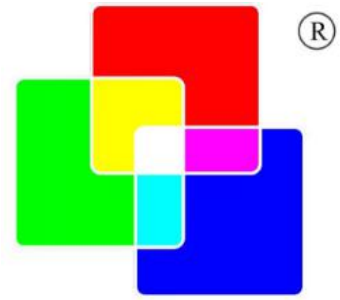
PREPARED BY : 制作人 ::HJW 日期：2024-12-19	 **EASYQUICK TECHNOLOGY** SPECIFICATION 深圳市易快来科技股份有限公司	SPEC No：（规格型号：） **EQT674BKU295G**
		FILE No ：（档案编号 ：） **EQ2024121901**
R&D APPROVED BY: 审核:GJM 日期：2024-12-19		ISSUE（日期） **2024-12-19**
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QC APPROVED BY: 确认：WPC 日期：2024-12-19		APPLICABLE DIVISION （适用范围） ■LCD DIVISION ■液晶模组

For **720*1600**TFT LCD Module Model No

EQT674BKU295G

SPEC

Customer side signature（客户方签名）			
签名 / 部门	Acknowled-ge（承认人）	Date（日期）	Remarks（备注）
Structure（结构）			
Electronics（电子）			
Item（项目）			
Quality（品质）			

EASYQUICK TECHNOLOGY

（易快来科技）

1. Application（应用）

This data sheet is to introduce the specification of **EQT674BKU295G** active matrix 16.7M color TFT LCD module.
Main color LCD module is controlled by Driver IC ICNL9916AC-02.
If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.
As to basic specification of driver IC refer to the IC specification and handbook.

本规格书是为了介绍 **EQT674BKU295G** 有源矩阵 16.7M 彩色 TFT LCD 模块的规格。
主彩色液晶显示模块由驱动芯片 ICNL9916AC-02 控制
本规范未尽事宜如有问题，双方必须认真协商解决。
驱动 IC 的基本规格参照《IC 规格书》和相关《手册》。

2. Construction and Outline （结构与大纲）

Construction: LCD panel, Driver (COG), FPC with electric components, 18 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.
There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.
In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.
So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

结构:液晶面板，驱动或 COG，带电子元件的 FPC, 18 个白光 LED 块，棱镜片，扩散器，导光器和反射器，塑料框架机械固定。
不应有可能影响显示功能的划痕、污迹、芯片、畸变等外部缺陷。
为了实现薄型模块结构，采用双面胶带固定液晶面板。由于这些胶带不能保证永久有效固定面板，LCD 面板在出厂时可能会从模块内移动。
所以在液晶模块组包装和进柜时，请务必将包装结构设计成用海绵等软材料支撑液晶面板的边缘。

3. Mechanical Specification（参数规格）

No.	Item	Contents	Unit
1	Screen size（屏幕尺寸）	6.745 inch	/
2	Display mode（显示模式）	Normally black	/
3	View Angle（视角）	FULL VIEW	/
4	Display format（分辨率）	720*1600	/
5	Outline Dimensions（外形尺寸）	74.37(W)×164.64(H)×2.15(D)	mm
6	Active area（ 显示范围）	70.308 (H)x 156.24 (V)	mm
7	Pixel size(像素）	0.09765×0.09765	mm
8	Interface type（接口类型）	MIPI 4 lane	/
9	Color Depth（颜色深度）	16.7M	/
10	Module power consumption（模组功耗）	148(LCD/90HZ)+1080（BL）	mW
11	Back light type（背光类型）	LED	/
12	Driver IC（驱动 IC）	ICNL9916AC-02	/
13	Weight（重量）	TBD	g

Note 1: Not include FPCs & Bezel extrude stucture.

备注 1: 不包括排线和面板构造

4. ABSOLUTE MAXIMUM RATINGS(绝对最高额定值)

Item	Symbol	Min.	Max.	Unit	Note
I/O logic voltage（I/O 逻辑电压）	IOVCC	-0.3	2	V	
Supply voltage（供电电压）	VSP	-0.3	6.6	V	
Supply voltage（供电电压）	VSN	0.3	-6.6	V	
Operation temperature（运行温度）	Top	-20	+70	°C	
Storage temperature（储存温度）	Tst	-30	+80	°C	

5. ELECTRICAL CHARACTERISTICS（电气特性）

5.1 TFT DC CHARACTERISTICS(at Ta=25°C)

TFT 直流特性(at Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply input voltage（电源输入电压）	VDD	-	-	-	V	
I/O logic voltage（I/O 逻辑电压）	VDDI	1.65	1.8	1.95	V	
Input voltage 'H' level（输入电压高水平）	VIH	0.7VDDI	-	VDDI	mV	
Input voltage 'L' level（输入电压低水平）	VIL	0	-	0.3VDDI	mV	
Power supply current （电源电流）	IVSP/IVSN	-	9	-	mA	
I/O logic voltage current （I/O 逻辑电压电流）	IVDDI	-	24	-	mA	
TFT gate on voltage （TFT门打开电压）/ Input positive voltage(输入正极电压）	VSP	4.5	5.8	6.5	V	
TFT gate off voltage （TFT门关闭电压）/ Input Negative voltage(输入负极电压）	VSN	-6.5	5.8	-4.5	V	
Analog power supply voltage（模拟电源电压）	AVDD	-	-	-	V	
TFT input common mode voltage （TFT输入共模电压）	VCOM	-	-	-	V	Note1

Note1 : The value is just the reference value. The customer can optimize the setting value by the different D-IC

Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..

备注：该值只是参考值，应用于不同的驱动芯片需要优化设定值，VCOM 必须进行调整来优化显示质量，比如串扰、对比度等

5. 2 LED back light（背光灯）

At main panel the back light uses 18 pcs edge light type white LED.
在背光的主面板用 18 颗白色 LED 灯

Table 4（表 4）

Parameter（参数）	Symbol（样品）	Min.（最小值）	Typ.（标准值）	Max.(最大值)	Unit（单位）	Remark（备注）
LED Voltage（LED 电压）	VLED	25.2	27	28.8	V	
LED Current（LED 电流）	ILED	-	40	-	mA	
Power Consumption（电功率）	WLED	-	1080	-	mW	
Connection Type(Serial/Parallel/Other) 连接类型(串联/并联/其他)		9S2P LEDs				

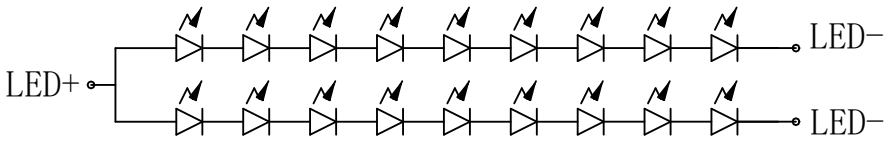
Note:

*18 pcs of LED

*Please consider Allowable Forward Current on used temperature

*18 颗灯

* 请考虑允许范围内的正向电流的使用温度



BACKLIGHT CIRCUIT

(If=20mA/LED , 2.7-2.9/LED)

Fig.1*Schematics drawing of lighting （绘制照明图 图.1）

6. Interface signals（接口信号）

TFT Module Interface description（TFT 模块接口描述）

Pin No.	Symbol	Description	Remark
1	LCM_LED-	BL LED K1	
2	LCM_LED+	BL LED A	
3	NC	NC	
4	NC	NC	
5	CTP_INT	CTP interrupt pin	
6	GND	Ground	
7	CTP_RST	CTP_RESET pin	
8	MDSI_DATA3_N	MIPI-DSI data Lane 3 negative-end pin.These pins are MIPI-DSI D3- differential data signals if MIPI interface is used	
9	LCM_TE	Output Pad for TE or checking signal	
10	MDSI_DATA3_P	MIPI-DSI data Lane 3 positive-end pin.These pins are MIPI-DSI D3+ differential data signals if MIPI interface is used	
11	LCM_RSTN	This signal will reset the function and must be applied to properly initialize	
12	GND	Ground	
13	TP_SPI1_CLK	Touch SPI clock	
14	MDSI_DATA2_N	MIPI-DSI data Lane 2 negative-end pin.These pins are MIPI-DSI D2- differential data signals if MIPI interface is used	
15	TP_SPI1_DI	Touch SPI data output	
16	MDSI_DATA2_P	MIPI-DSI data Lane 2 positive-end pin.These pins are MIPI-DSI D2+ differential data signals if MIPI interface is used	
17	TP_SPI1_DO	Touch SPI data input	
18	GND	Ground	
19	TP_SPI1_CSN	Touch SPI chip selection	
20	MDSI_CLK_N	MIPI-DSI clock Lane negative-end input pin.These pins are MIPI-DSI CLK- differential clock signals if MIPI interface is used.HS_CN are differential small amplitude signals.	
21	LCD_CABC	Backlight on/off control. This pin can be connected to external LED driver IC	
22	MDSI_CLK_P	MIPI-DSI clock Lane positive-end input pin.These pins are MIPI-DSI CLK+ differential clock signals if MIPI interface is used.HS_CP are differential small amplitude signals.	
23	VDD1V85	Power supply for logic power and I/O circuit.	
24	GND	Ground	

25	LCD_ID(GND)	ID=GND	
26	MDSI_DATA1_N	MIPI-DSI data Lane 1 negative-end input pin.These pins are MIPI-DSI D1- differential data signals if MIPI interface is used.	
27	NC	NC	
28	MDSI_DATA1_P	MIPI-DSI data Lane 1 positive-end input pin.These pins are MIPI-DSI D1+ differential data signals if MIPI interface is used.	
29	LCM_AVEE	5.8V Power supply to analog circuits pin	
30	GND	Ground	
31	NC	NC	
32	MDSI_DATA0_N	MIPI-DSI data Lane 0 negative-end pin.These pins are MIPI-DSI D0- differential data signals if MIPI interface is used	
33	LCM_AVDD	5.8V Power supply to analog circuits pin	
34	MDSI_DATA0_P	MIPI-DSI data Lane 0 positive-end pin.These pins are MIPI-DSI D0+ differential data signals if MIPI interface is used	
35	GND	Ground	
36	GND	Ground	
37	GND	Ground	
38	GND	Ground	
39	GND	Ground	
40	GND	Ground	
39	GND	Ground	
40	GND	Ground	

7. AC CHARACTERISTICS（交流特性）

4.4、 MIPI AC Timings Characteristics

4.4.1 Vertical Timings for DSI video mode

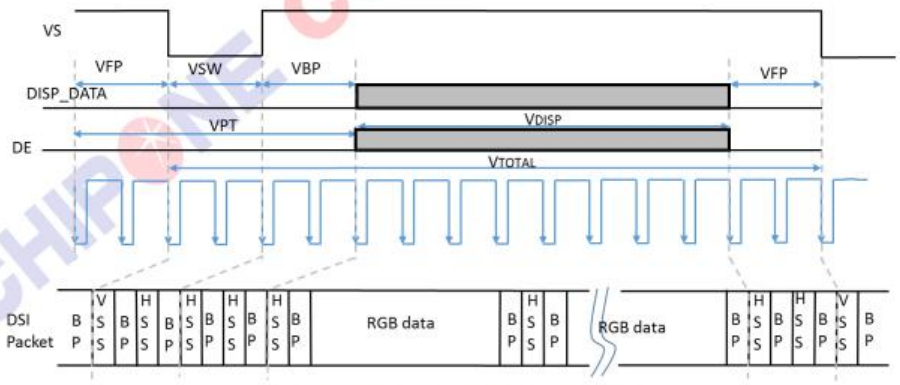


Figure 4. Vertical timings for DSI interface

Table 17. Vertical Timings List for DSI video mode

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Vertical Total	VTOTAL					Line	1
Vertical low pulse width	VSW		2	4		Line	2
Vertical front porch	VFP		4	16		Line	1
Vertical back porch	VBP		4	16		Line	2
Vertical data start point		VSW+VBP	6	20		Line	2
Vertical blanking period	VPT	VSW+VBP+VFP	10			Line	
Vertical active area	VDISP		-	1600	1760	Line	
Vertical Frame rate	VFR			60	120	Hz	

Condition : Ta =25℃,Resolution = 720(RGB)* 1600

Note 1: ICNL9916 support long-VFP LFR mode.

Note 2: The VSW and VBP pulse width are related to GSP and GCK timing. The GSP and GCK must be set at corresponding position for LCM normal display.

4.4.2 Horizontal Timings for DSI video mode

Figure 5. Horizontal timings for DSI video mode

Table 18. Horizontal Timings List for DSI video mode

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
HS low pulse width	HSW		0.2			uS	
Horizontal back porch	HBP		0.2			uS	
Horizontal front porch	HFP		0.3			uS	
Horizontal data start point		HSW+HBP	0.4			uS	
Horizontal blanking period	HBLK	HSW+HBP+HFP	0.7			uS	
Horizontal active area	HDISP				720	DCLK	

Condition : Ta =25℃,Resolution = 720(RGB)* 1600.

4.5、MIPI AC Characteristics

4.5.1 High Speed Mode – Clock Timings

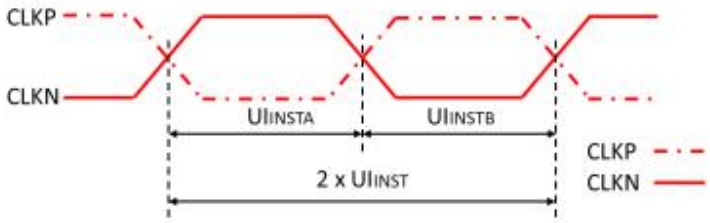


Figure 6. Clock Timing

Table 19. High Speed Mode – Clock Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CLK P/N	$2xUI_{INST}$	Double UI instantaneous	1.66		25	nS	
CLK P/N	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	0.83		12.5	nS	1

Note 1: UI = UI_{INSTA} = UI_{INSTB}.

4.5.2 High Speed Mode – Clock / Data Timings

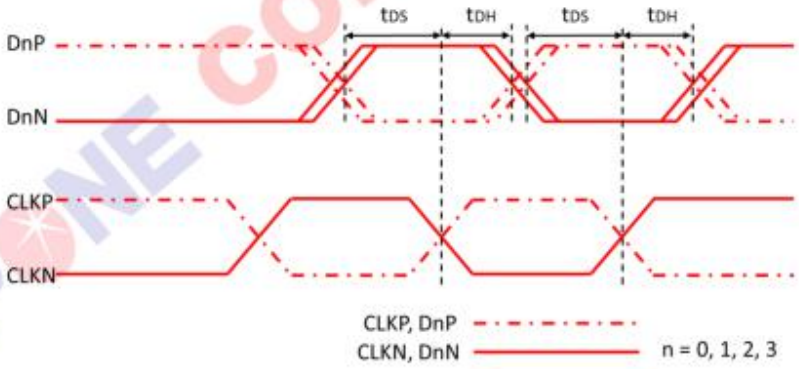


Figure 7. DSI Clock / Data Timings

Table 20. High Speed Mode – Clock / Data Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
Dn P/N (n=0,1,2 and 3)	t_{DS}	Data to Clock Setup time	0.15*UI			UI	
	t_{DH}	Clock to Data Hold time	0.15*UI			UI	

4.5.3 High Speed Mode – Rising and Falling Timings

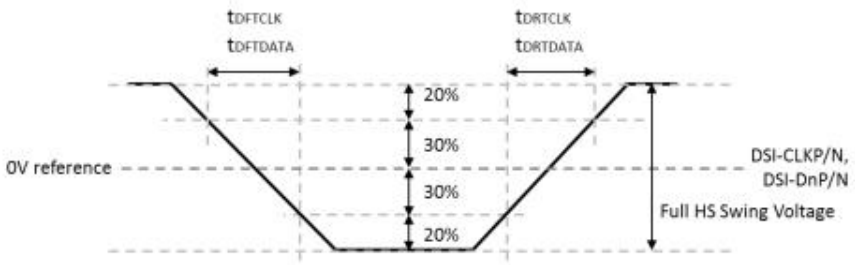


Figure 8. Rising and Falling Timings

Table 21. High Speed Mode – Rising and Falling Timing

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N	150pS		0.3*UI		1,2,3
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N	150pS		0.3*UI		1,2,3

Note 1: DnP/N, n =0,1,2 and 3.
Note 2: The display module has to meet timing requirements, which are defined for the transmitter (AP) on MIPI D-PHY standard.
Note 3: DSI-CLK+ = CLKP.
DSI-CLK- =CLKN.
DSI-D0+ =D0P.
DSI-D0- =D0N.

4.5.4 Low Speed Mode – Bus Turn Around

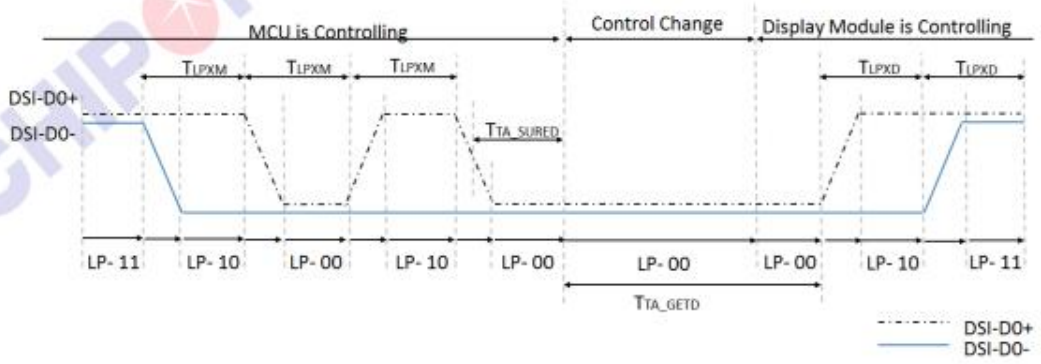


Figure 9. Bus Turnaround (BTA) from AP to display module Timing

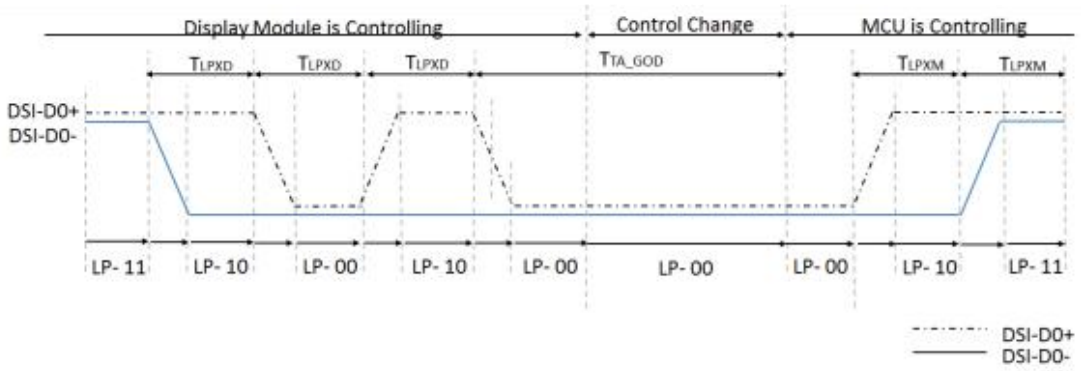


Figure 10. Turnaround (BTA) from Display module to AP Timing

Table 22. Low Speed Mode – Bus Turn Around Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	T_{LPXM}	Length of LP-00,LP-01,LP-10 or LP11 periods AP to Display Module	50		75	nS	1
D0P/N	T_{LPXD}	Length of LP-00,LP-01,LP-10 or LP11 periods Display Module to AP	50		75	nS	1
D0P/N	T_{TA_SURED}	Time-out before the Display Module starts driving	T_{LPXD}		2* T_{LPXD}	nS	1
D0P/N	T_{TA_GETD}	Time to drive LP-00 by Display Module	5* T_{LPXD}			nS	1
D0P/N	T_{TA_GOD}	Time to drive LP-00 after turnaround request –AP	4 * T_{LPXD}			nS	1

Note 1: D0P = DSI-D0+, D0N = DSI-D0-.

4.5.5 Data Lanes from Low Power Mode to High Speed Mode

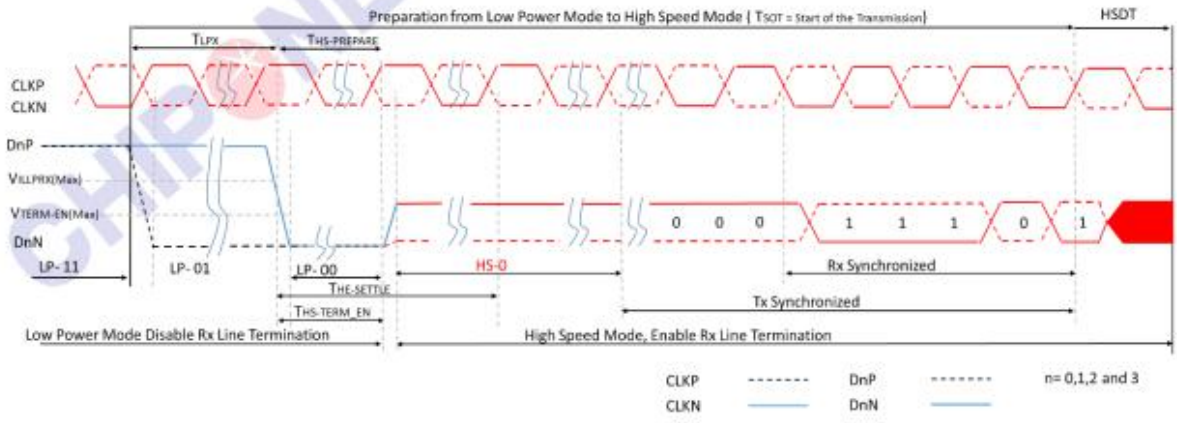


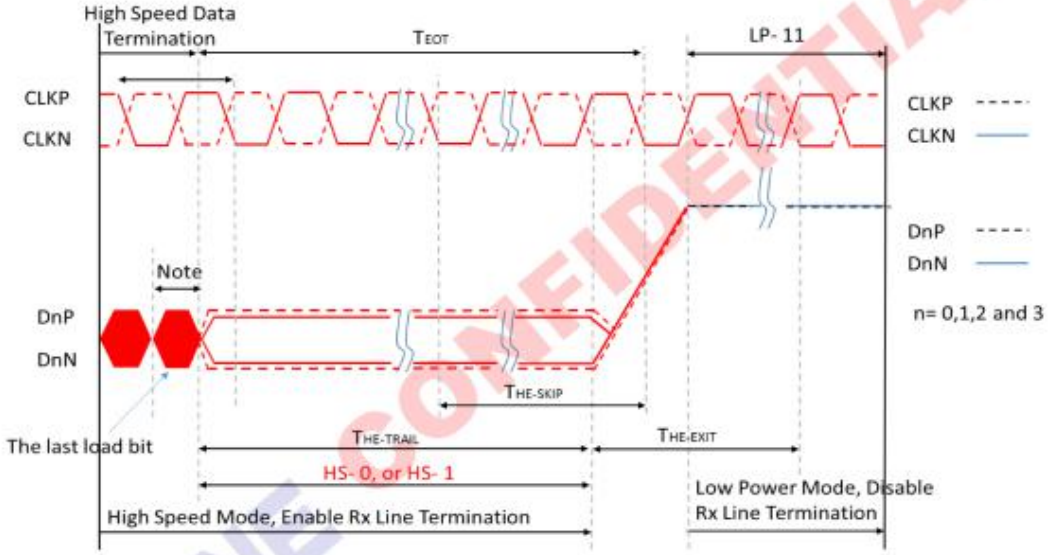
Figure 11. Data Lanes from High Speed Mode to Low Power Mode Timing

Table 23. Data Lanes from Low Power Mode to High Speed Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	T_{LPX}	Length of any Low Power State Period	50			nS	1
DnP/N	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
DnP/N	$T_{HS-TREM-EN}$	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

Note 1: DnP/N, n=0,1,2 and 3.

4.5.6 Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

Figure 12. Data Lanes from High Speed Mode to Low Power Mode Timing

Table 24. Data Lanes from High Speed Mode to Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	$T_{HS-SKIP}$	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
DnP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			nS	1

Note 1: DnP/N, n=0,1,2 and 3.

4.5.7 DSI Clock Burst – High speed mode to /from Low Power Mode

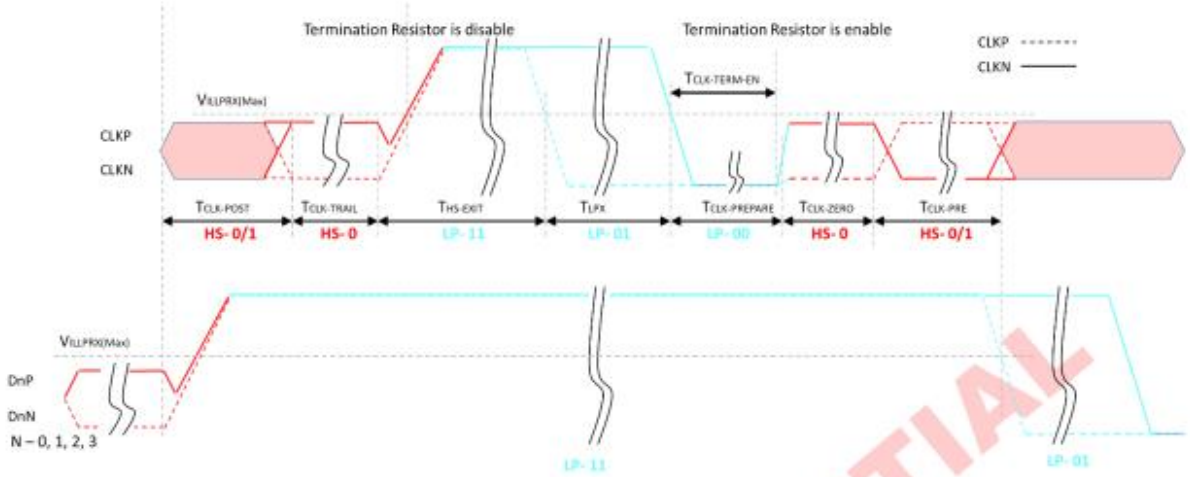


Figure 13. Clock Lane –High speed mode to / from Low Power Mode Timing

Table 25. DSI Clock Burst – High speed mode to /from Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CKP/N	$T_{CLK-POST}$	Time that the AP shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52*UI			nS	
CKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			nS	
CKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination			38	nS	
CKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300			nS	
CKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8*UI			nS	

4.7、SPI AC Characteristics

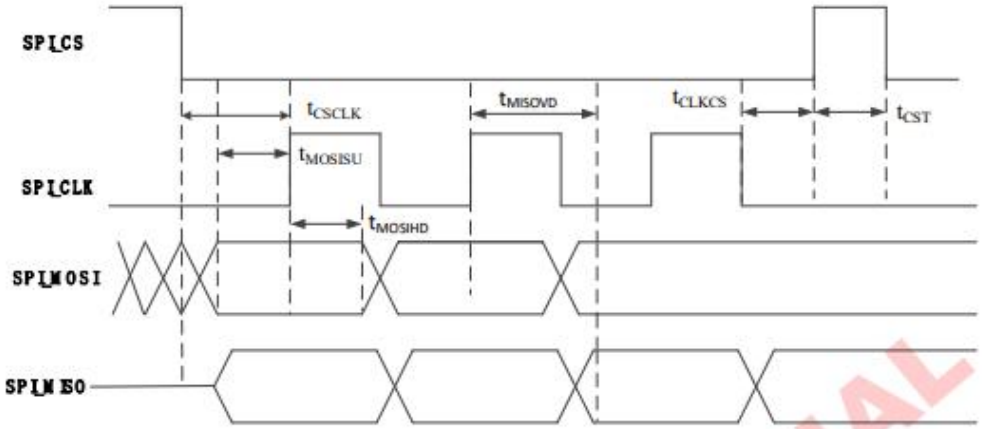


Figure 15. AC and DC Characteristics of the I/O stages for SPI-bus

Table 28. Characteristics of the I/O stages for SPI-bus

Symbol	Parameter	Specification			Unit	Notes
		Min.	Typ.	Max.		
VIL	Digital input low voltage	-0.3		0.3*IOVCC	V	
VIH	Digital input high voltage	0.7*IOVCC		IOVCC	V	
VOL	Digital low output voltage			0.3*IOVCC	V	
VOH	Digital high output voltage	0.7*IOVCC			V	
IIL	Input leakage		1		nA	

Table 29. Characteristics of the I/O lines for SPI-bus

Symbol	Parameter	Specification		Unit	Notes
		Min.	Max.		
t_{MISOVD}	SPI_MISO valid time		50	ns	
t_{MOSISU}	SPI_MOSI setup time	15		ns	
t_{MOSIHD}	SPI_MOSI hold time	15		ns	
t_{CSCLK}	Time for SPI_CS low to SPI_CLK high	100		ns	
t_{CLKCS}	Time for SPI_CLK low to SPI_CS high	100		ns	
t_{CST}	Minimum SPI_CS high time before setting SPI_CS low.	2		us	
$f_{SPI,CLK}$	SPI_CLK Frequency		16	MHz	

4.8、Reset Input Timing

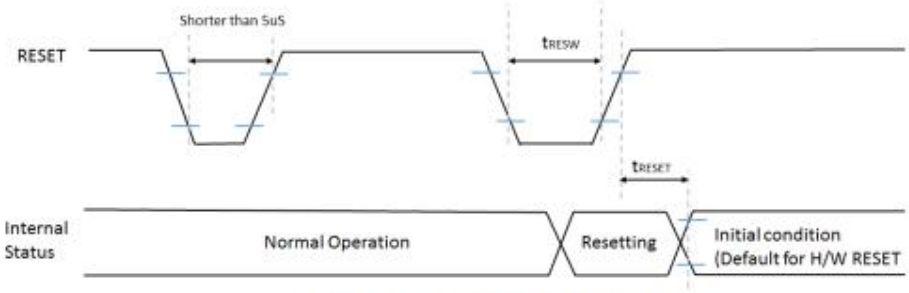


Figure 16. Reset Input Timing

Table 30. Reset Input Timing

Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	t_{RESW}	Reset "L" pulse width		10			μS	1
	t_{RESET}	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	2

Condition : Ta =25℃.

Note 1: Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.

Table 31. Reset Input Actions

RESET Pulse	Action
Short than 5us	Reset Rejected
Long than 10μS	Reset
Between 5us and 10μS	Reset Start

Note 2: During the resetting period, the display will work on blanking states (The display is entering blanking sequence, which maximum time is 120ms, when Reset starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

Note 3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time (tRESET) within 5ms after a rising edge of RESET.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below.

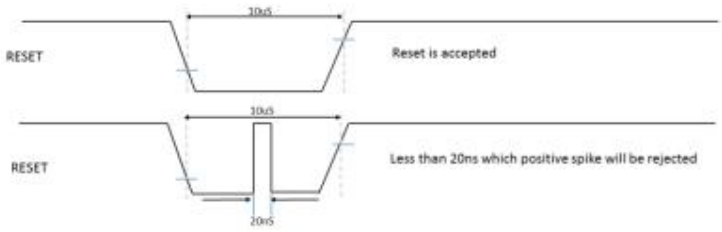


Figure 17. Reset rejection Timing

Note 5: It is necessary to wait 5ms after releasing RESET before sending any commands.

8. POWER SEQUENCE（电源时序）

7.2、 Power ON Sequence

7.2.1 3 power mode (PCCS=0)

If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VSP and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10μsec after both VSP and IOVCC have been applied.

The power on sequence for different power input modes are shown below tables and figures.

For External Flash

Table 62. Power ON Sequence Timing for External Flash

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
Ton1	IOVCC on to VSP on delay.	>0.1			ms	
Ton2	VSP on to VSN on delay.	>0			us	
T1	IOVCC power rise time.	0.05		2	ms	
T2	VSP power rise time.	0.2			ms	
T3	VSN power fall time.	0.2			ms	
T4	3power ready to RESET_N high.	10			ms	
T5	HS_VCC to MIPI bus ready delay.	0			ms	Note1
T6	RESET_N low period.	10			us	
T7	RESET_N high to OTP load ready	30			ms	Note2
T9	Sleep-out command received to video packet transmit delay.	-	120		ms	Note3
T10	Sleep-out command received to display on command transmit delay.	>0			ms	

Note1: T5 max time = TON1+T2+TON2+T3+T4

Note2: In general, flash reload time needs 20ms. If external flash application is necessary, T7 needs more than 30ms for OTP and flash reload. The MIPI commands should be transmitted after T7.

Note3: The 120 ms is the recommend time of T9 by default setting. If 70 ms is required, it has to working on particular register setting.

The Power on sequence is shown as below.

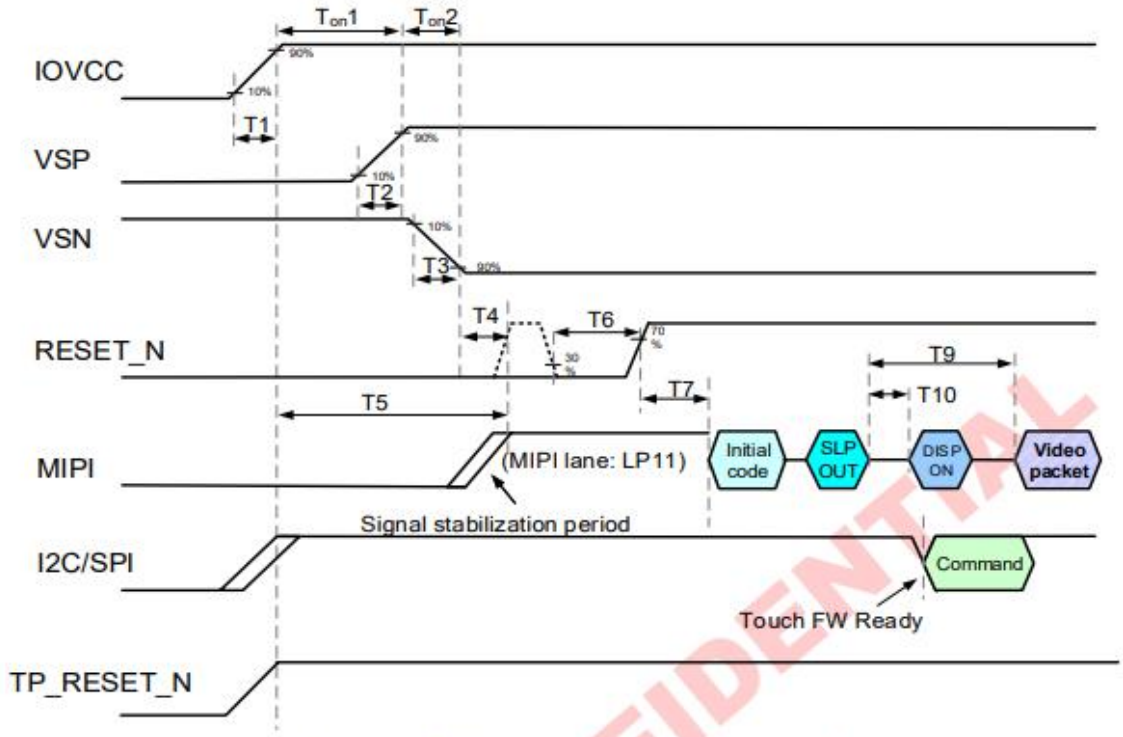


Figure 109. Power on sequence for External Flash

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Note2: This power-on sequence is based on adding Schottky diode on VGL pin to ground.

Note3: TP_RESET_N is recommended keeps high all the times.

For Host download (Zero-Flash)

Table 63. Power ON Sequence Timing for Host download (Zero-Flash)

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
Ton1	IOVCC on to VSP on delay.	>0.1			ms	
Ton2	VSP on to VSN on delay.	>0			us	
T1	IOVCC power rise time.	0.05		2	ms	
T2	VSP power rise time.	0.2			ms	
T3	VSN power fall time.	0.2			ms	
T4	3power ready to RESET_N high.	10			ms	
T5	HS_VCC to MIPI bus ready delay.	0			ms	Note1
T6	RESET_N low period.	10			us	
T7	RESET_N high to OTP load ready	30			ms	Note2
T9	Sleep-out command received to video packet transmit delay.	-	120		ms	Note3
T10	Sleep-out command received to display on command transmit delay.	>0			ms	

Note1: T5 max time = TON1+T2+TON2+T3+T4

Note2: In general, flash reload time needs 20ms. If external flash application is necessary, T7 needs more than 30ms for OTP and flash reload. The MIPI commands should be transmitted after T7.

Note3: The 120 ms is the recommend time of T9 by default setting. If 70 ms is required, it has to working on particular register setting.

The Power on sequence is shown as below.

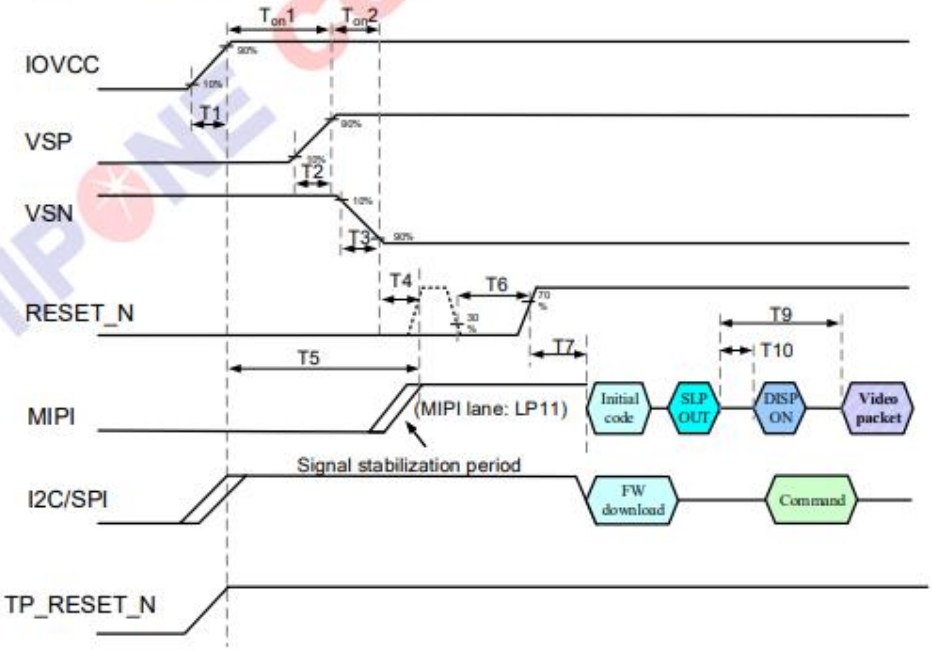


Figure 110. Power on sequence for Host Download (Zero-Flash)

9. Optical Characteristics（光学特征）

Item 项目		Symbol（样品）	Condition（条件）	Min.（最小值）	Typ.（标准值）	Max.（最大值）	Unit（单位）	Remark（备注）
Response time（响应时间）	Rise（上升）+Fall（下降）	Tr +Tf	θ=0°	-	-	30	ms	Note 1 FIG.1
Luminance（亮度）		Br	θ=0°	400	450	-	Cd/m^2	Note 3 FIG.2
Luminance uniformity（亮度均匀性）		YU	θ=0°	80	-	-	%	Note 4 FIG.2
Contrast ratio（对比度）		CR	θ=0°	1000	1500	-	-	Note 2 FIG.2
Viewing angle(with Polarizer)（视角）	Top（顶部）		CR≥10	75	80	-	degree	Note 6 FIG.3
	Bottom（底部）			75	80	-		
	Left（左边）			75	80	-		
	Right（右边）			75	80	-		
White Chromaticity（白色色度）		X	CIE	-0.03	0.30	+0.03	-	Note 5 FIG.2 CIE1931
		Y		-0.03	0.32	+0.03	-	
NTSC（色彩饱和度）			-	TBD	-	-	%	Note 5 FIG.2

Note1. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state.Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%.

And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

Note2.Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula.

For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

Measured at the center area of the LCD

Note3.Definition of surface luminance

Surface luminance is the luminance with all pixels displaying white.

For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note4.Definition of luminance uniformity

The luminance uniformity in surface luminance is det-ermined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$Yu = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.

For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON's BM-5or BM-7 photo detector or compatible.

FIG.1. The definition of response Time

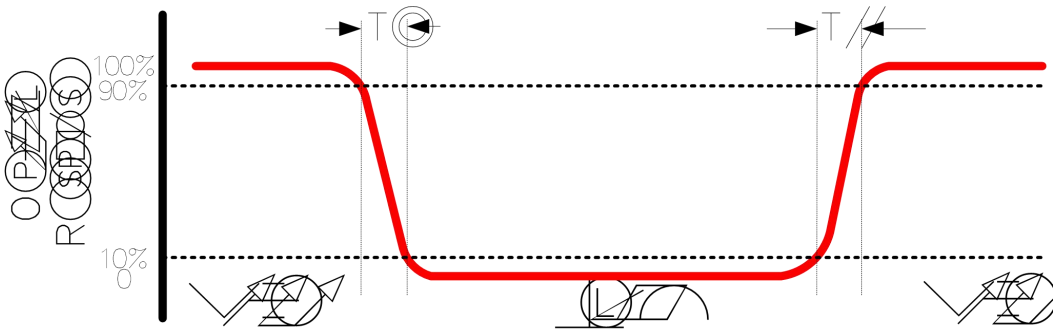


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

H,V : Active area

Light spot size ∅=1.5mm (BM-7)50cm distance or compatible distance from the LCM surface to detector lens.

Test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-7 or compatible ,see Figure b.

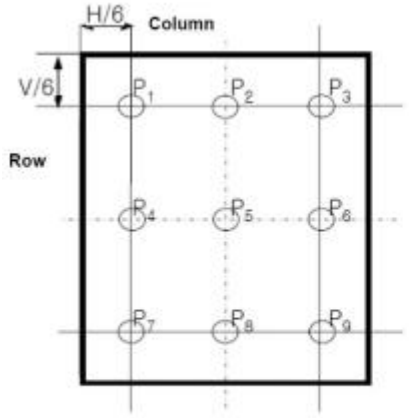


Figure a

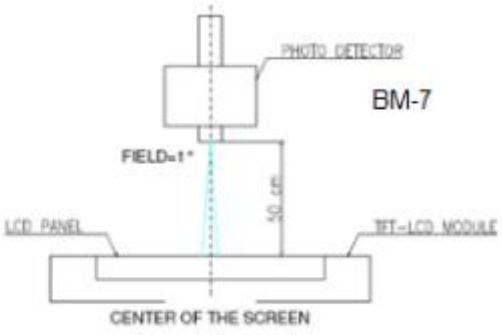
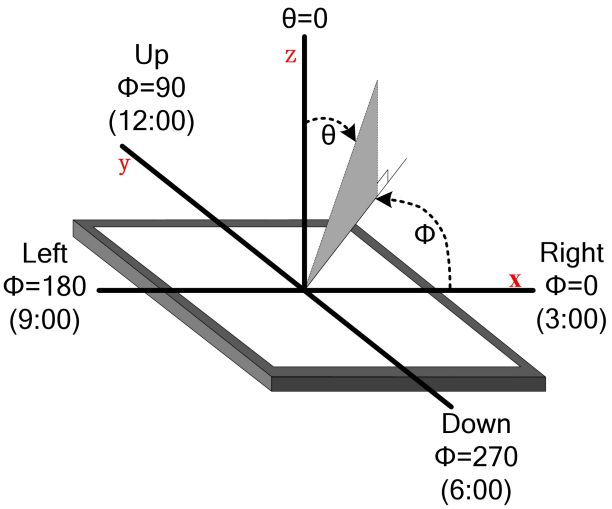
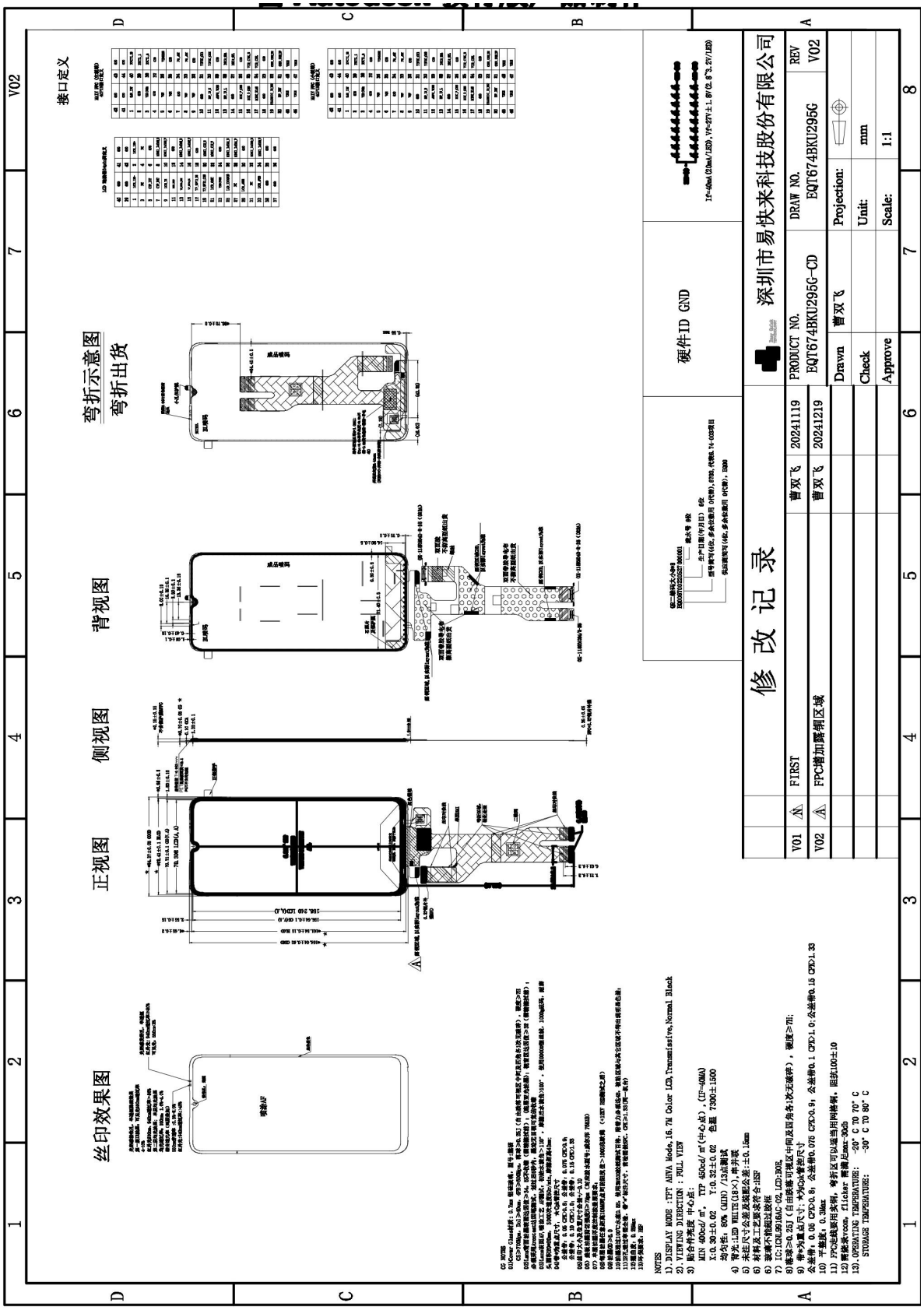


Figure b

FIG.3. The definition of viewing angle



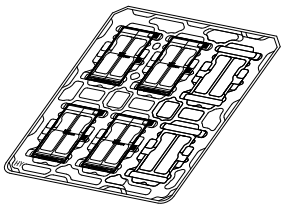
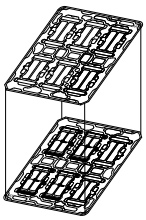
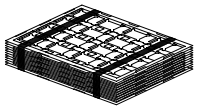
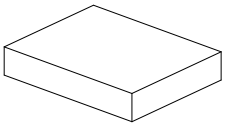
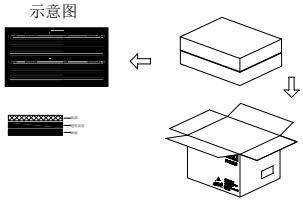
10.LCD Module Outline dimensions （模组外形图 ）



11.Packaging Specification（包装规格）

1.1 Package quantity in one Box : TBD PCS
1.2 Box Size : TBD mm * TBD mm * TBD mm
1.3 1 BOX = TBD CARTON
1.4 1 CARTON = TBD (Full tray) + 1 (dummy / top tray) =TBD tray
1.5 1 TRAY = TBD PCS LCM

注：此为示意图

<table>
<tr>
<td>(1) 模块平放入吸塑盘内，
每盘放6PCS产品
  </td>
<td>(2)吸塑盘交叉叠放
  </td>
<td>(3)十盘加一个空盘共10x6=60pcs
吸塑盘交叉叠放后用胶袋和胶纸打包
叠放次序
B
C
A
C
B
C
A
  </td>
</tr>
<tr>
<td>(4)真空包装
将打包好的产品装进包装袋并抽真空密封，
  </td>
<td>(5) 产品装箱
先在纸箱底下放一个纸板，让后放一小包产品进去，在放一个纸板在上面，最后在放一个纸板在上面，二包叠加装箱
示意图
  </td>
<td>(6) 封箱
外箱标签中须体现供应商名称、EQ料号及包装数量。
 
外箱标签贴于侧面
数量：2x60=120 PCS/箱</td>
</tr>
</table>