For　**1080*2340**TFT LCD Module Model No

EQT630BRD343G
SPEC

Customer side signature（客户方签名）			
部门　　　　签名	Acknowled-ge （承认人）	Date（日期）	Remarks（备注）
Structure （结构）			
Electronics （电子）			
Item （项目）			
Quality （品质）			

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1. Application（应用）

This data sheet is to introduce the specification of **EQT630BRD343G** active matrix 16.7M color TFT   LCD module.

Main color LCD module is controlled by Driver IC   TD4330**.**

If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.

As to basic specification of driver IC refer to the IC specification and handbook.

本规格书是为了介绍 **EQT630BRD343G** 有源矩阵 16.7M 彩色 TFT LCD 模块的规格。

主彩色液晶显示模块由驱动芯片 TD4330 控制

本规范未尽事宜如有问题，双方必须认真协商解决。

驱动 IC 的基本规格参照《IC 规格书》和相关《手册》。

2. Construction and Outline （结构与大纲）

Construction: LCD panel, Driver (COG), FPC with electric components, 18 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.

In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.

So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

结构:液晶面板，驱动或 COG，带电子元件的 FPC, 18 个白光 LED 块，棱镜片，扩散器，导光器和反射器，塑料框架机械固定。

不应有可能影响显示功能的划痕、污迹、芯片、畸变等外部缺陷。

为了实现薄型模块结构，采用双面胶带固定液晶面板。由于这些胶带不能保证永久有效固定面板，LCD 面板在出厂时可能会从模块内移动。

所以在液晶模块组包装和进柜时，请务必将包装结构设计成用海绵等软材料支撑液晶面板的边缘。

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3. Mechanical Specification（参数规格）

No.	Item	Contents	Unit
1	Screen size（屏幕尺寸）	6.3 inch	/
2	Display mode（显示模式）	Normally black	/
3	View Angle（视角）	FULL VIEW	/
4	Display format（分辨率）	1080*2340	/
5	Outline Dimensions（外形尺寸）	72.90(W)×157.15(H)×2.29(D)	mm
6	Active area（ 显示范围）	67.07(H)×145.31(V)	mm
7	Pixel size(像素）	0.0207(H) x 0.0621 (V)	mm
8	Interface type（接口类型）	MIPI 4 lane	/
9	Color Depth（颜色深度）	16.7M	/
10	Module power consumption（模组功耗）	TBD	W
11	Back light type（背光类型）	LED	/
12	Driver IC（驱动 IC）	TD4330	/
13	Weight（重量）	TBD	G

Note 1: Not include FPCs & Bezel extrude stucture.

备注 1: 不包括排线和面板构造

4. ABSOLUTE MAXIMUM RATINGS(绝对最高额定值)

Item	Symbol	Min.	Max.	Unit	Note
I/O logic voltage（I/O 逻辑电压）	IOVCC	-0.3	2.3	V	
Supply voltage（供电电压）	VSP	-0.3	6.2	V	
Supply voltage（供电电压）	VSN	-6.2	0.3	V	
Operation temperature（运行温度）	Top	-20	+70	°C	
Storage temperature（储存温度）	Tst	-30	+80	°C	

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5. ELECTRICAL CHARACTERISTICS（电气特性）

5.1 TFT DC CHARACTERISTICS(at Ta=25°C)

TFT 直流特性(at Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply input voltage（电源输入电压）	VDD	-	-	-	V	
I/O logic voltage（I/O 逻辑电压）	VDDIO	1.65	1.8	1.95	V	
Input voltage 'H' level（输入电压高水平）	VIH	0.7VDDIO	-	VDDIO	mV	
Input voltage 'L' level（输入电压低水平）	VIL	0	-	0.3VDDIO	mV	
Power supply current （电源电流）	IVDD	-	-	-	mA	
I/O logic voltage current （I/O 逻辑电压电流）	IVDDIO	-	TBD	-	mA	
TFT gate on voltage （TFT门打开电压）/ Input positive voltage(输入正极电压）	AVDD	4.5	5.6	6.0	V	
TFT gate off voltage （TFT门关闭电压）/ Input Negative voltage(输入负极电压）	AVEE	-6.0	-5.6	-4.5	V	
TFT input common mode voltage （TFT输入共模电压）	VCOM	-	-	-	V	Note1

Note1 : The value is just the reference value. The customer can optimize the setting value by the different D-IC

Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..

备注：该值只是参考值，应用于不同的驱动芯片需要优化设定值，VCOM 必须进行调整来优化显示质量，比如串扰、对比度等

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5. 2 LED back light（背光灯）

At main panel the back light uses 18 pcs edge light type white LED.

在背光的主面板用 18 颗白色 LED 灯

Table 4（表 4）

Parameter（参数）	Symbol（样品）	Min.（最小值）	Typ.（标准值）	Max.（最大值）	Unit（单位）	Remark（备注）
LED Voltage（LED 电压）	VLED	25.2	27	28.8	V	
LED Current（LED 电流）	ILED	-	40	-	mA	
Power Consumption（电功率）	WLED	-	1080	-	mW	
Connection Type(Serial/Parallel/Other) 连接类型(串联/并联/其他)	9S2P LEDs					

Note:

*18 pcs of LED

*Please consider Allowable Forward Current on used temperature
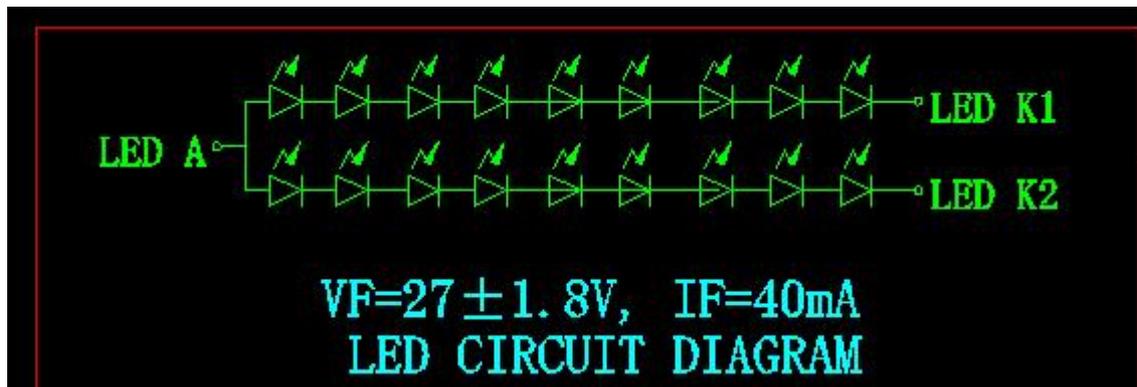
*18 颗灯

* 请考虑允许范围内的正向电流的使用温度

Fig.1*Schematics drawing of lighting （绘制照明图 图.1）

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6. Interface signals（接口信号）

Pin No.	LCD 接口 pin 定义	LCD 接口说明
1	GND	地
2	D3P	MIPI_数据线
3	D3N	MIPI_数据线
4	GND	地
5	D2P	MIPI_数据线
6	D2N	MIPI_数据线
7	GND	地
8	D1P	MIPI_数据线
9	D1N	MIPI_数据线
10	GND	地
11	D0P	MIPI_数据线
12	D0N	MIPI_数据线
13	GND	地
14	TCP	MIPI_时序线
15	TCN	MIPI_时序线
16	GND	地
17	GND	地
18	GND	地
19	GND	地
20	GND	地
21	GND	地
22	VDDIO_1.8V	电源=1.8V
23	AVDD_5.8V	电源=+5.8V
24	AVEE_-5.8V	电源=-5.8V
25	LEDK1	背光负极 1
26	LEDK2	背光负极 2
27	LEDA	背光正极
28	GND	地
29	GND	地
30	LCD_RESET	LCD 复位
31	LCD_TE	LCD_TE
32	GND	地
33	LCD_ID(NC)	NC
34	I2C_SCL	TP 时序=1.8V
35	I2C_SDA	TP 数据=1.8V

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36	TP_RESET	TP 复位=1.8V
37	TP_INT	TP 中断=1.8V
38	GND	地
39	TP_IOVCC	NC
40	TP_VCC(3.0V)	NC

7. AC CHARACTERISTICS（交流特性）

Table 32. DC characteristics

Item		Symbol	Unit	Test Condition	Minimum	Typical	Maximum
DSI-2 D Option current consumption (DPHYVCC-GND) (D option)	High-speed (HS) mode	I_{HS}	mA	IOVCC = 1.800V, DPHYVCC = 1.800V, DSI-2 4 lanes, fDSICLK = 675 MHz, DSI-2 data: 24'h000000 Ta = 25 °C	–	–	10 (TBD)
	Low power (LP) mode	I_{LP}	µA	IOVCC = 1.800V, DPHYVCC = 1.800V, Clock lane = LP11, Data lane = LP11, Ta = 25 °C	–	–	250 (TBD)
	Deep Standby mode	I_{DST_DP}	µA	IOVCC = 1.800V, DPHYVCC = 1.800V, Ta = 25 °C	–	1 (TBD)	5 (TBD)
DSI-2 C Option current consumption (DPHYVCC-GND) (C option)	High-speed (HS) mode	I_{HS}	mA	IOVCC = 1.800V, DPHYVCC = 1.800V, DSI-2 3 lanes, SYMBOL RATE = 1.2Gsps, DSI-2 data: 24'h000000 Ta = 25 °C	–	–	TBD
	Low power (LP) mode	I_{LP}	µA	IOVCC = 1.800V, DPHYVCC = 1.800V, Clock lane = LP111, Data lane = LP111, Ta = 25 °C	–	–	TBD
	Deep Standby mode	I_{DST_DP}	µA	IOVCC = 1.800V, DPHYVCC = 1.800V, Ta = 25 °C	–	TBD	TBD

17.4. Step-up Circuit Characteristics

Table 33. Step-up circuit characteristics

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
Step-up output voltage	VGH	V	Ta = 25 °C, VSP = 5.60V, VSN = -5.60V, VC2 = 4'hC, VC3 = 4'h9, VLM2 = 6'h14, BT2 = 1'h0, Iload = -3 mA (TBD)	7.60 (TBD)	8.00 (TBD)	–
	VGL	V	Ta = 25 °C, VSP = 5.60V, VSN = -5.60V, VC2 = 4'hC, VC3 = 4'h9, VLM3 = 6'h14, BT3 = 1'h0, Iload = +3 mA (TBD)	–	-8.00 (TBD)	-7.60 (TBD)

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17.5. Clock Characteristics

Table 34. Clock characteristics

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
Oscillation clock	fosc	MHz	IOVCC = 1.8V	67.9 (TBD)	70.0 (TBD)	72.1 (TBD)

17.6. Reset Timing Characteristics

Table 35. Reset timing characteristics

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
Reset low-level width1	tRW1	µs	Power supply on	3000 (TBD)	–	–
Reset low-level width2	tRW2	µs	Operation	1000 (TBD)	–	–
Reset low-level width3	tRW3	µs	Power supply on	0 (TBD)	–	–
Reset low-level width4	tRW4	µs	Power supply on	0 (TBD)	–	–
Reset time (Sleep IN)	tRT1	ms	–	–	–	20 (TBD)
Noise reject width	tRESNR	µs	–	–	–	1 (TBD)
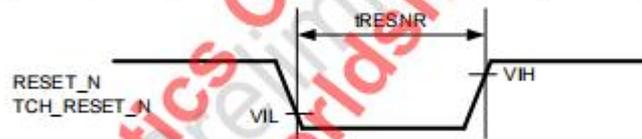
Figure 16. Reset reject pulse width
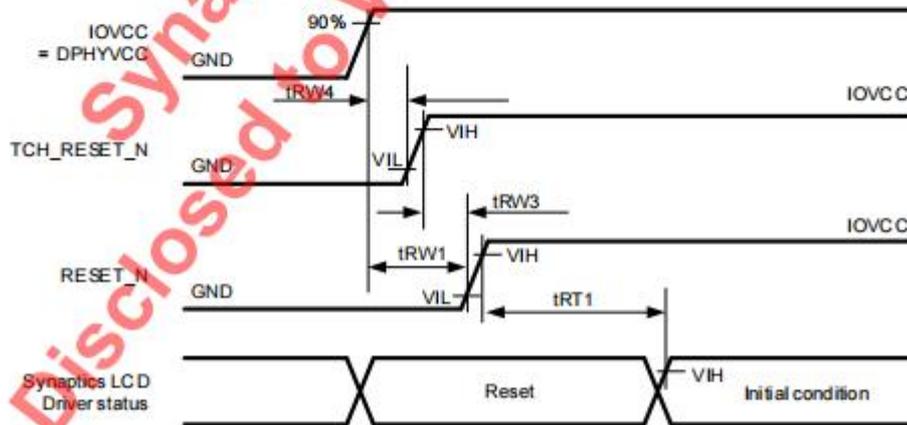
Figure 17. Reset timing characteristics at power supply on
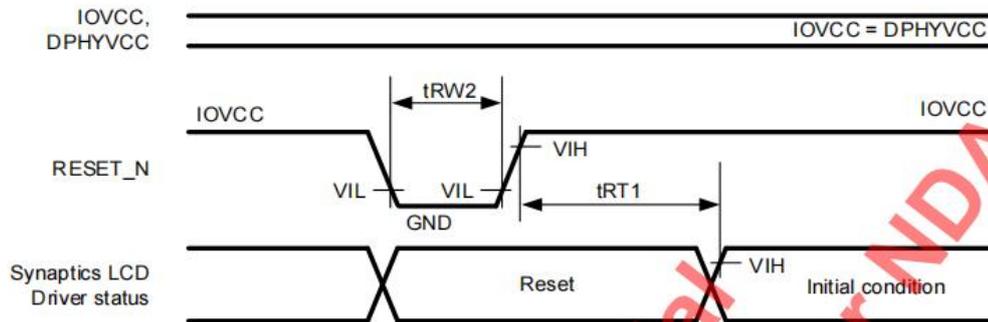
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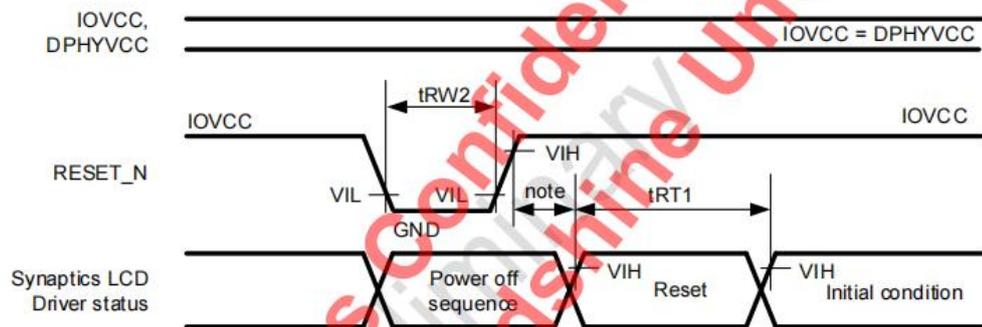

Figure 18. Reset timing in Sleep In

Figure 19. Reset timing in Sleep Out

Note: Ask your Synaptics sales representative for a custom datasheet appendix for details of the power on/off sequence.

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Table 36. Liquid crystal driver output characteristics

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
Source driver output delay time*	tdds	µs	IOVCC = 1.8V, , Ta = 25 °C, VSP = 5.60V, VSN = -5.60V, Reached voltage: defined grayscale voltage ±35 mV VPL = 7'h2B, VNL = 7'h2B Load resister R = 4 kΩ Load capacitance C = 30 pF	–	–	1.2 (TBD)

* The LCD driver output delay time depends on the load on the liquid crystal panel. Therefore, the frame frequency and one-line cycle must be specified. Check the image quality on the panel to be used.
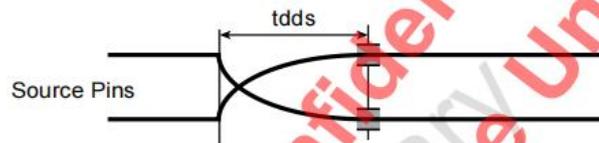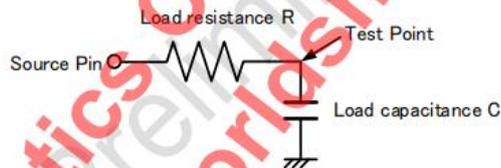

Figure 20. Liquid crystal driver output timing

Figure 21. Load circuit for testing LCD driver output characteristics

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17.8. MIPI D-PHY Characteristics

Table 37. MIPI D-PHY characteristics

	Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
HS-RX	Differential input high threshold	VIDTH	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	–	–	70
	Differential input low threshold	VIDTL	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	-70	–	–
	Single-ended input low voltage	VILHS	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	-40	–	–
	Single-ended input high voltage	VIHHS	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	–	–	460
	Common-mode voltage HS receive mode[1]	VCMRX(DC)	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	70	–	330
	Differential input impedance[2]	ZID	Ω	IOVCC = DPHYVCC = 1.65V ~ 1.95V	–	100	–
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	-50	–	550
	Logic 1 input voltage	VIH	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	880	–	1350
	I/O leakage current	ILEAK	µA	Vin = -50 mV ~ 1350 mV	-10	–	10
LP-TX	Thevenin output low level	VOL	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	-50	–	50
	Thevenin output high level	VOH	V	IOVCC = DPHYVCC = 1.65V ~ 1.95V	1.1	1.2	1.3
	Output impedance of LP transmitter[2]	ZOLP	Ω	IOVCC = DPHYVCC = 1.65V ~ 1.95V	110	–	–
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	–	–	200
	Logic 1 contention threshold	VIHCD	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	450	–	–

1. VCMRX (DC) = (VDP + VDN)/2
2. Excluding COG resistance (contact resistance and ITO wiring resistance).

Table 38. MIPI D-PHY host characteristics

	Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
HS-TX	Differential output voltage	|VOD|	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	140	200	270

Note: This SPEC is the HS-TX SPEC. Use the host in conformity with this specification.

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17.8.1. MIPI D-PHY HS-RX Clock and Data-Clock Specifications

Table 39. MIPI D-PHY HS-RX clock and data-clock specifications

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum	Footnote
DSICLK frequency	fDSICLK	MHz	IOVCC = DPHYVCC = 1.65 ~ 1.95V	250	—	675	1
DSICLK cycle time	tCLKP	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	1.6	—	4	1
DSI data transfer rate	tDSIR	Mbps	IOVCC = DPHYVCC = 1.65 ~ 1.95V	500	—	1350	1
Data to clock setup time	tSETUP	UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate ≦1000Mbps	0.15	—	—	1, 3
		ns		0.15	—	—	1, 2, 3
		UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate >1000Mbps	0.2	—	—	1, 3
		ns		0.15	—	—	1, 2, 3
Clock to data hold time	tHOLD	UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate ≦1000Mbps	0.15	—	—	1, 3
		ns		0.15	—	—	1, 2, 3
		UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate >1000Mbps	0.2	—	—	1, 3
		ns		0.15	—	—	1, 2, 3

1. Minimum 110 mV/-110 mV HS differential swing is required for display data transfer.
2. tSETUP/tHOLD Time are measured without HS-TX Jitter.
3. Minimum tSETUP/tHOLD Time is 0.15 UI or 0.20 UI. This value may change according to the DSI transfer rate.

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Table 40. MIPI D-PHY LP-RX/TX clock and data-clock specifications

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	40 ns + 4 • UI	–	85 ns + 6 • UI
$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	145 ns + 10 • UI	–	–
Time to drive flipped differential state after last payload data bit of a HS transmission burst[1, 2]	$T_{HS-TRAIL}$	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	Maximum (n • 8 • UI, 60 ns + n • 4 • UI)	–	–
Time to drive LP-11 after a HS burst	$T_{HS-EXIT}$	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	100	–	–
Time to drive LP-00 after a turnaround request	T_{TA-GO}	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	4 • T_{LPTX}		
Time that the new TX waits after the LP-10 state before transmitting the bridge state (LP-00) during a link turnaround	$T_{TA-SURE}$	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	1 • T_{LPTX}	–	2 • T_{LPTX}
Time that the new TX drives the bridge state (LP-00) after accepting control during a link turnaround	T_{TA-GET}	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	5 • T_{LPTX}		
Length of any low-power state period	T_{LPX}	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	50	–	–
Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between the master and slave sides	Ratio T_{LPX}	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	2/3	–	3/2
Time that the transmitter continues sending HS clock after the last associated data lane has transitioned to LP mode[3]	$T_{CLK-POST}$	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	60 ns + 52 UI	–	–
$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting the clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	300	–	–
Time that the HS clock is driven prior to any associated data lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V	8	–	–
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	38	–	95
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	60	–	–
Time from the start of THS-TRAIL period to the start of the LP-11 state[2]	T_{EOT}	–	IOVCC = DPHYVCC = 1.65 ~ 1.95V	–	–	105 ns + n • 12 • UI
Length of the low-power TX state period when using the DSI-2 clock[4, 5]	T_{LPTX1}	UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V	–	1/fTXCLK	–
Length of the low-power TX state period when using the internal OSC clock[4, 5]	T_{LPTX2}	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	–	4/fosc	–

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1. If a > b then max (a, b) = a, otherwise max (a, b) = b
2. Where n = 1 for forward direction HS mode.
3. TD4330 works with this specification, although the last part of the internal process remains when the clock lane enters LP-11 and TD4330 works without the remaining process if tCLK-POST is more than 512 UI.
4. TD4330 uses the DSI-2 clock from the host processor if the DSI-2 clock lane is active, and uses the internal oscillator clock if the DSI-2 clock lane is stopped.
5. See section 22.6 (DSI-2 Control Section (B6h) (D-PHY')) in this document for more information about the DSITXDIV register function.
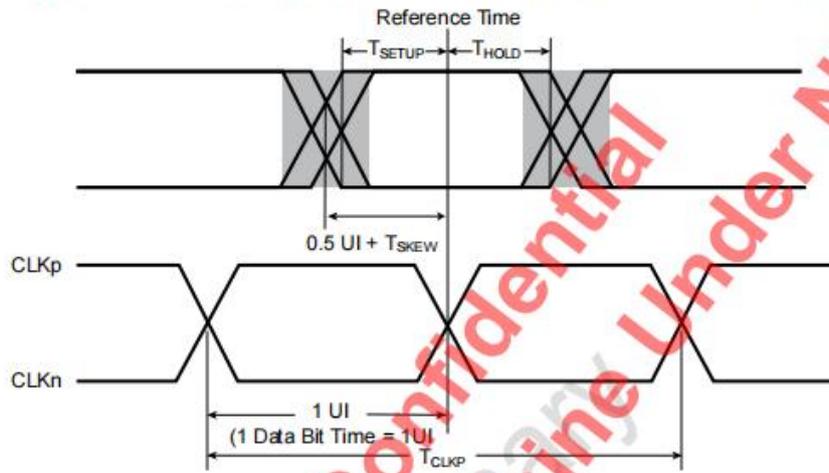

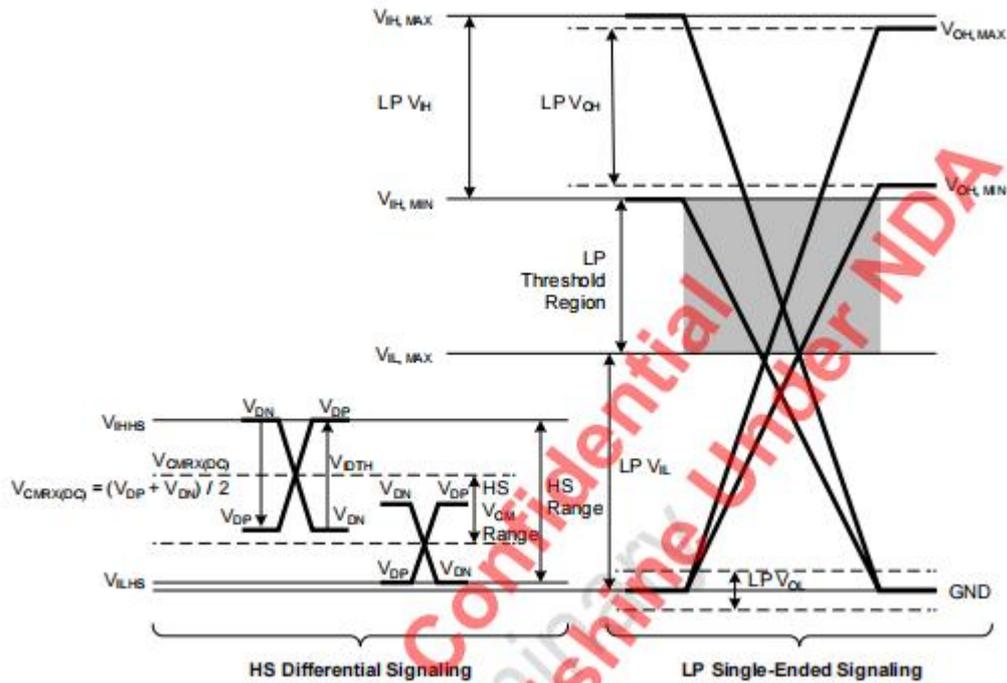Figure 22. Data to clock timing definitions [1]
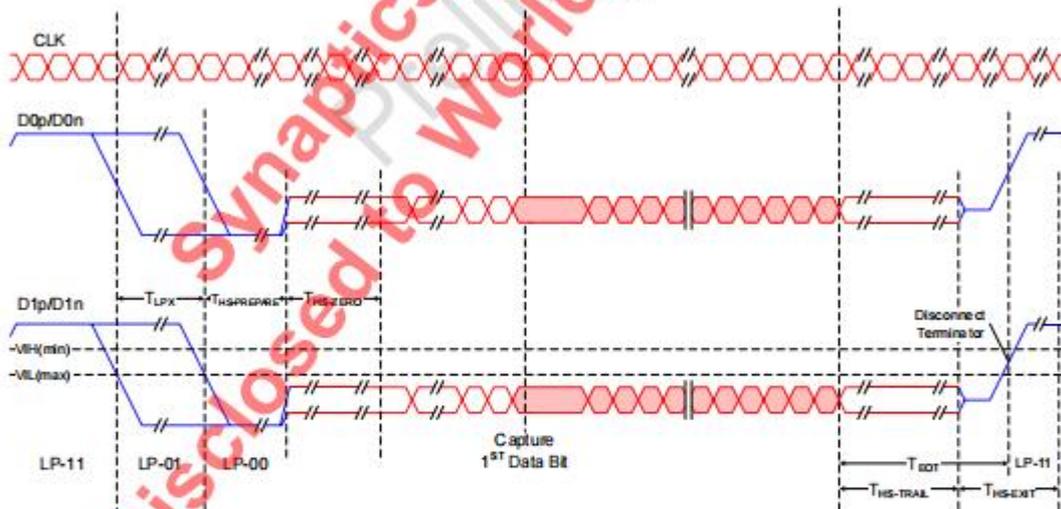
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Figure 23. D-PHY LP mode[2]

Figure 24. HS data transmission in bursts[3]

[2] MIPI Alliance Standard for D-PHY, Version 1.1 7-November-2011
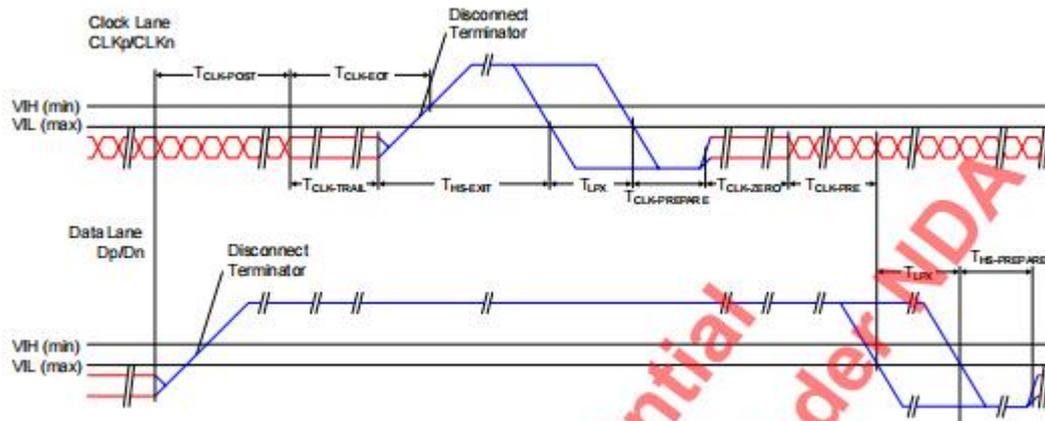[3] MIPI Alliance Standard for D-PHY, Version 1.1 7-November-2011

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Figure 25. Switching the clock lane between clock transmission and LP mode[4]

Figure 26. D-PHY LP mode

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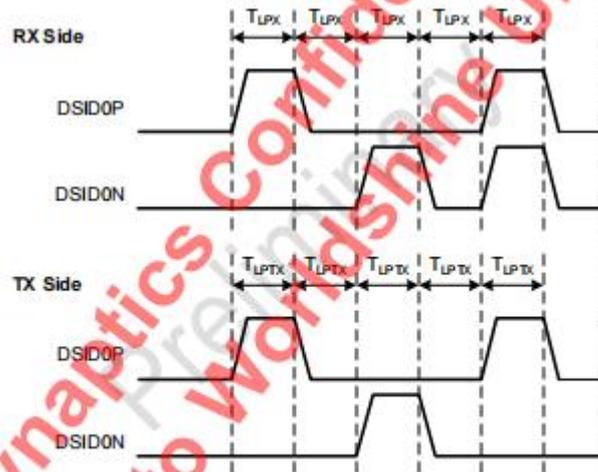
8. POWER SEQUENCE（电源时序）

14. Supply On/Off Timing Specifications

TD4330 can be operated by supplying the VSP and VSN power supplies directly.
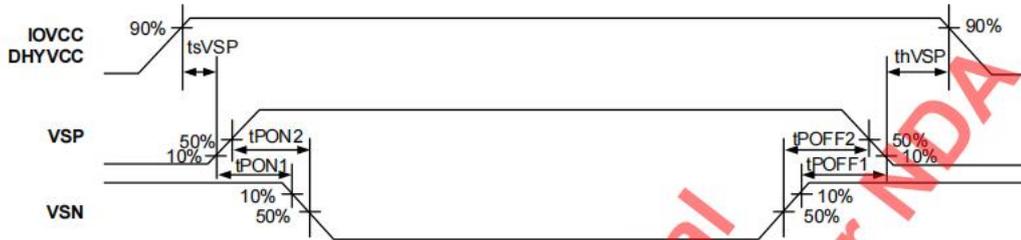
Figure 14. Power supply on/off timing

Table 26. Power supply specifications

Item	Symbol	Unit	Test Condition	Minimum	Maximum
VSP-VSN delay time (10% to 10%)	tPON1	µs	Power on	0	—
VSP-VSN delay time (50% to 50%)	tPON2	µs	Power on	0	—
System power on to VSP ON time	tsVSP	ms	Power on	1	—
VSN-VSP delay time (10% to 10%)	tPOFF1	µs	Power off	0	—
VSN-VSP delay time (50% to 50%)	tPOFF2	µs	Power off	0	—
VSP OFF to system power off time	thVSP	µs	Power off	0	—

Note: For reset timing information, see section 17.6 (Reset Timing Characteristics) in this document.

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9. Optical Characteristics（光学特征）

Item 项目		Symbol（样品）	Condition（条件）	Min.（最小值）	Typ.（标准值）	Max.（最大值）	Unit（单位）	Remark（备注）
Response time（响应时间）	Rise（上升）+Fall（下降）	Tr+Tf	θ=0°	-	25	35	ms	Note 1 FIG.1
Luminance（亮度）		Br	θ=0°	420	450	-	Cd/m²	Note 3 FIG.2
Luminance uniformity（亮度均匀性）		YU	θ=0°	-	80	-	%	Note 4 FIG.2
Contrast ratio（对比度）		CR	θ=0°	1000	1500	-	-	Note 2 FIG.2
Viewing angle(with Polarizer)（视角）	Top（顶部）		CR≥10	70	80	-	degree	Note 6 FIG.3
	Bottom（底部）			70	80	-		
	Left（左边）			70	80	-		
	Right（右边）			70	80	-		
White Chromaticity（白色色度）	X		CIE	0.265	0.295	0.325	-	Note 5 FIG.2 CIE1931
	Y			0.285	0.315	0.345	-	
NTSC（色彩饱和度）			-	-	71	-	%	Note 5 FIG.2

Note1. Definition of response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black"state.Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%.

And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

Note2.Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula.

For more information see FIG.2.

Contrast ratio= $\dfrac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$

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Measured at the center area of the LCD

Note3.Definition of surface luminance

Surface luminance is the luminance with all pixels displaying white.

For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note4.Definition of luminance uniformity

The luminance uniformity in surface luminance is det-ermined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$Yu = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,......,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,......,Pn)}}$$

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.

For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON's BM-5or BM-7 photo detector or compatible.

FIG.1. The definition of response Time
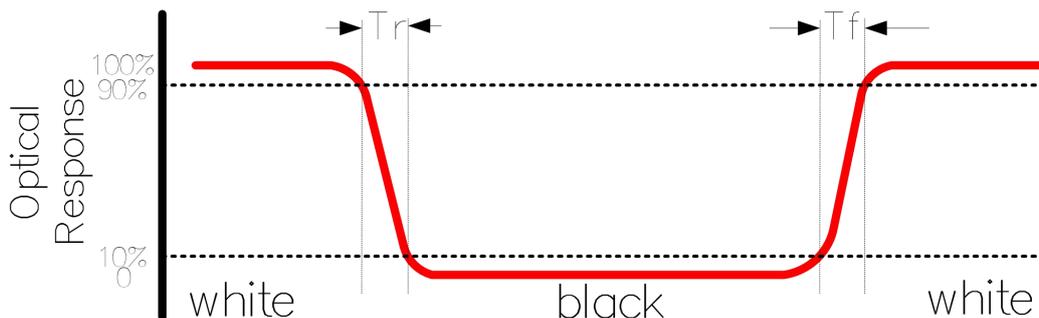
FIG.2. Measuring method for contrast ratio, surface luminance,
luminance uniformity, CIE (x,y) chromaticity

H,V : Active area

Light spot size $\varnothing$ =1.5mm (BM-7)50cm distance or compatible distance from the LCM surface to detector lens.

Test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-7 or compatible ,see Figure b.
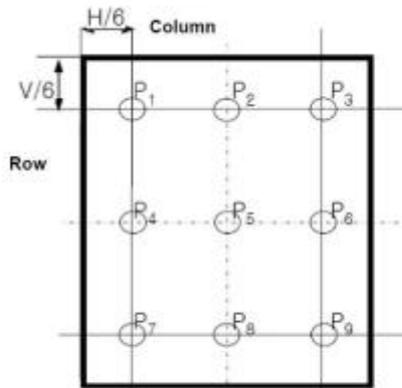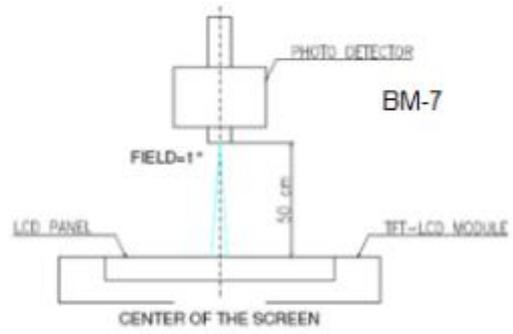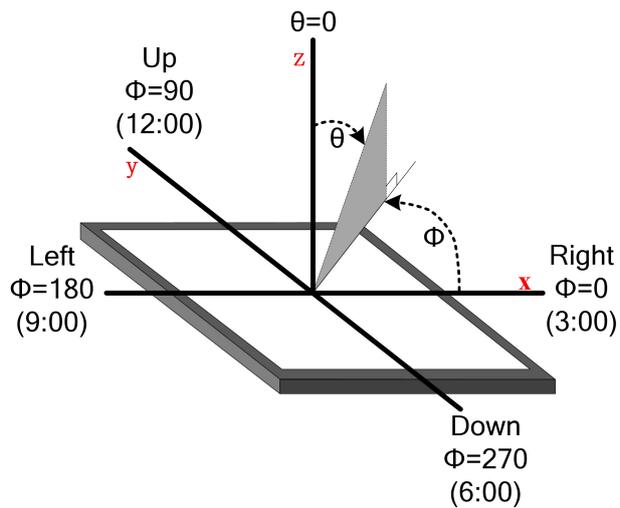
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Figure a

Figure b

FIG.3. The definition of viewing angle

10. **LCD Module Outline dimensions** （模组外形图）

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丝印效果图

正视图　側视图　背视图

弯折示意图
弯折出货

LCM接口定义

No.	信号
1	GND
2	D3P
3	D3N
4	GND
5	D2P
6	D2N
7	GND
8	D1P
9	D1N
10	D0P
11	D0N
12	GND
13	TCP
14	TCN
15	GND
16	GND
17	GND
18	GND
19	GND
20	GND
21	GND
22	VDDIO_1.8V
23	AVDD_5.8V
24	AVEE_-5.8V
25	LEDK1
26	LEDK2
27	LEDA
28	GND
29	GND
30	LCD_RESET
31	LCD_TE
32	GND
33	LCD_ID(NC)
34	I2C_SCL(1.8V)
35	I2C_SDA(1.8V)
36	TP_RESET(1.8V)
37	TP_INT(1.8V)
38	GND
39	TP_IOVCC(NC)
40	TP_VCC(3.0V)(NC)

IR孔: 蓝紫色IR油墨
550nm可见光透过率:15%±5%
850nm红外光透过率:＞80%

黑色
镀AF

6.3 Inch
1080x2340
AILL

CG关键参数技术要求：
1. 产品结构：2D；
2. 玻璃材质：0.7mm /康宁三代，镀AF膜；
3. CS≥750Mpa，DOL≥40 um，CT≤67 MPa，表面硬度≥7H(1KG)
4. 落球冲击：60g/50cm,高度自由跌落四周+中心点共5点 各一次不破，实验后盖板外观、机械功能正常；
5. Lens油墨区域表面能≥32，（Arcotest Dyne测试笔，酒精擦拭后，5S收缩小于10%）
6. 油墨绝缘阻抗值≥1000MΩ/10mm按客户要求，在ECG背面油墨区选择上下左右量测4点；
7. CG油墨的不透明性（OD值）：OD≥5.0
8. CG视窗透过率≥90%；雾度(Haze)≤2%；
9. 油墨附着力：丝印区域（除镜面银）百格后用3M胶/610胶粘贴以90°反拉3次，要求达到 ISO 等级 1 或ASTM 等级 4B：在切口的相交处有小片剥落，划格区内实际破损≤5%
10. 操作温度：-30°C TO 70°C，储存温度：-40°C TO 80°C；
11. TP翘曲度≤0.3mm；

NOTES
1. DISPLAY MODE :TFT AHVA Mode,16.7M Color LCD,Transmissive,Normal Black
2. VIEWING DIRECTION : FULL VIEW
3. BACKLIGHT:18CHIP-WHITE LED
4. OPERATING TEMPERATURE: -20°C TO 70°C
   STORAGE TEMPERATURE: -30°C TO 80°C
5. 产品符合RoHS2.0&HF&REACH标准
6. IF=40mA , LUMINANCE(中心点):With TP 420 cd/m2(min.),450 cd/m2(typ.)
   色坐标范围(中心值)：X=0.295±0.03 Y=0.315±0.03
7. IC:TD4330 LCD:BOE 6.3寸 FHD+
Gamma: 2.2±0.3; Crosstalk: 3.0%(max); Flicker: -25DB Max.;
8. TEST Connector:亚奇OK-14F040-04
9.
10. 绕线OTP VCOM
11. 带 * 的尺寸为关键尺寸,带（）为参考尺寸；
12. 未注公差:±0.15；
13. 总成平整度≤0.3mm
14. 产品仅支持MIPI VIDEO MODE

IR保护膜
带颜色撕手

BL喷码区域

总成喷码区域

导电布上下对位参考此条压印电缆
单面带胶粘接相正常高度 0.8,
压框后≥0.5

漏铜(GND)
根据实际走胶调整

双面带胶导电布 T=0.05mm

亚奇：
OK-14MO40-04

FOG段 导电布T=0.05

对位线

双面EMI接地

铜片补强(GND)T=0.2mm,
FPC+铜片补强=0.35±0.05

弯折软化区

元件高+高温胶导电布 T=0.9MAX
FPC+焊锡高度+胶布T=0.45mm
组装段导电布覆盖
FOG段导电布重叠一小部分
机壳注意避空

组装段 导电布T=0.05

FOG段 导电布T=0.05

VF=27±1.8V, IF=40mA
LED CIRCUIT DIAGRAM

LED A+ LED K1 LED K2

修 改 记 录

| V01 | ⚠ | NEW(在6.3-008G基础上更换IC,LCD型号) | 曹双飞 | 20250211 |

深圳市易快来科技股份有限公司

PRODUCT NO. EQT630BRD343G-CD	DRAW NO. EQT630BRD343G	REV V01
Drawn 曹双飞 20250211	Projection:	
Check	Unit: mm	
Approve	Scale: 1:1	

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11.　Packaging Specification（包装规格）

1.1　Package quantity in one Box :　TBD　PCS

1.2　Box Size : TBD mm * TBD mm * TBD mm

1.3　1 BOX = TBD CARTON

1.4　1 CARTON = TBD (Full tray) + 1 (dummy / top tray) =TBD tray

1.5　1 TRAY = TBD PCS LCM

注：此为示意图
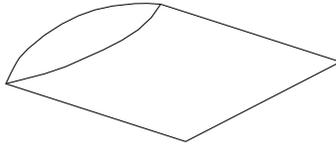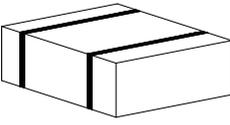
1.将产品放入吸塑盘内，每盘放 X PCS产品	2.将吸塑盘叠放在一起，N+1(空盘)，两端用胶带固定	3.将打包好的吸塑放入到包装袋中
4.将包装袋固定好为一小包，根据客户要求选择是否贴标签	5.产品装箱，先在纸箱底部放一层纸板，接着放入1包产品，在包装好的产品上再放一层纸板，然后再放入一包打包好的产品，最后盖上一张纸板后封箱	6.封箱后在外箱侧面贴外箱标签