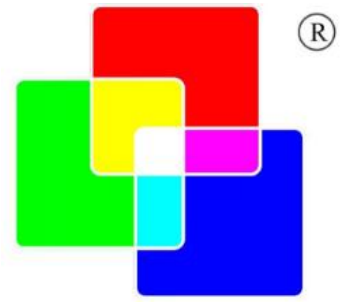
PREPARED BY : 制作人 :ZFG 日期：2025-06-30	 **EASYQUICK TECHNOLOGY** SPECIFICATION 深圳市易快来科技股份有限公司	SPEC No：（规格型号：） **EQT242BQZ384G**
R&D APPROVED BY: 审核:GJM 日期：2025-06-30		FILE No ：（档案编号 ：） **EQ2025063001** ISSUE（日期） **2025-06-30** PAGE（页码） 19
QC APPROVED BY: 确认：WSL 日期：2025-06-30		APPLICABLE DIVISION （适用范围） ■LCD DIVISION ■液晶模组

For **240*400** TFT LCD Module Model No

EQT242BQZ384G

SPEC

Customer side signature（客户方签名）			
签名 / 部门	Acknowled-ge（承认人）	Date（日期）	Remarks（备注）
Structure（结构）			
Electronics（电子）			
Item（项目）			
Quality（品质）			

EASYQUICK TECHNOLOGY

（易快来科技）

1. Application（应用）

This data sheet is to introduce the specification of **EQT242BQZ384G** active matrix 16.7M color TFT　LCD module.
Main color LCD module is controlled by Driver IC ST7796,Touch IC CST3530.
If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.
As to basic specification of driver IC refer to the IC specification and handbook.

本规格书是为了介绍 **EQT242BQZ384G** 有源矩阵 16.7M 彩色 TFT LCD 模块的规格。
主彩色液晶显示模块由驱动芯片 ST7796,控制,触控芯片　CST3530。
本规范未尽事宜如有问题，双方必须认真协商解决。
驱动 IC 的基本规格参照《IC 规格书》和相关《手册》。

2. Construction and Outline （结构与大纲）

Construction: LCD panel, Driver (COG), FPC with electric components, 6 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.
There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.
In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.
So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

结构:液晶面板，驱动或 COG，带电子元件的 FPC, 6 个白光 LED 块，棱镜片，扩散器，导光器和反射器，塑料框架机械固定。
不应有可能影响显示功能的划痕、污迹、芯片、畸变等外部缺陷。
为了实现薄型模块结构，采用双面胶带固定液晶面板。由于这些胶带不能保证永久有效固定面板，LCD 面板在出厂时可能会从模块内移动。
所以在液晶模块组包装和进柜时，请务必将包装结构设计成用海绵等软材料支撑液晶面板的边缘。

3. Mechanical Specification（参数规格）

No.	Item	Contents	Unit
1	Screen size（屏幕尺寸）	2.42 inch	/
2	Display mode（显示模式）	Normally black	/
3	View Angle（视角）	FULL VIEW	/
4	Display format（分辨率）	240*400	/
5	Outline Dimensions（外形尺寸）	41.03(W)×67(H)×2.85(D)	mm
6	LCD Active area（LCD 显示范围）	31.68(H)×52.8(V)	mm
7	Cover Viewe area（盖板可视范围）	31.18(H)×52.3(V)	
8	Pixel size(像素）	0.132 (H) x 0.132 (V)	mm
9	Interface type（接口类型）	MIPI	/
10	Color Depth（颜色深度）	16.7M	/
11	Module power consumption（模组功耗）	0.5	W
12	Back light type（背光类型）	LED	/
13	Driver IC（驱动 IC）	ST7796 CST3530	/
14	Weight（重量）	13.78	G
15	Gsensor IC	da218E	/

Note 1: Not include FPCs & Bezel extrude stucture.

备注 1: 不包括排线和面板构造

4. ABSOLUTE MAXIMUM RATINGS(绝对最高额定值)

Item	Symbol	Min.	Max.	Unit	Note
Power supply input voltage for TFT（TFT 电源输入电压）	VDD	-0.3	4.6	V	
Operation temperature（运行温度）	Top	-20	+70	°C	
Storage temperature（储存温度）	Tst	-30	+80	°C	

5. ELECTRICAL CHARACTERISTICS（电气特性）

5.1 TFT DC CHARACTERISTICS(at Ta=25°C)

TFT 直流特性(at Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply input voltage（电源输入电压）	VDD	2.5	2.75	3.3	V	
I/O logic voltage（I/O 逻辑电压）	VDDIO	-	-	-	V	
Input voltage 'H' level（输入电压高水平）	VIH	0.7VDD	-	VDD	V	
Input voltage 'L' level（输入电压低水平）	VIL	GND	-	0.3VDD	V	
Power supply current （电源电流）	IVDD	-	19	-	mA	
I/O logic voltage current （I/O 逻辑电压电流）	IVDDIO	-	-	-	mA	
TFT gate on voltage （TFT门打开电压）/ Input positive voltage(输入正极电压）	VGH/VSP	-	-	-	V	
TFT gate off voltage （TFT门关闭电压）/ Input Negative voltage(输入负极电压）	VGL/VSN	-	-	-	V	
Analog power supply voltage（模拟电源电压）	AVDD	-	-	-	V	
TFT input common mode voltage （TFT输入共模电压）	VCOM	-	-	-	V	Note1

Note1 : The value is just the reference value. The customer can optimize the setting value by the different D-IC

Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..

备注：该值只是参考值，应用于不同的驱动芯片需要优化设定值，VCOM 必须进行调整来优化显示质量，比如串扰、对比度等

5. 2 LED back light（背光灯）

At main panel the back light uses 6 pcs edge light type white LED.
在背光的主面板用 6 颗白色 LED 灯

Table 4（表 4）

Parameter（参数）	Symbol（样品）	Min.（最小值）	Typ.（标准值）	Max.(最大值)	Unit（单位）	Remark（备注）
LED Voltage（LED 电压）	VLED	16.8	18.3	19.8	V	
LED Current（LED 电流）	ILED	-	20	-	mA	
Power Consumption（电功率）	WLED	-	366	-	mW	
Connection Type(Serial/Parallel/Other) 连接类型(串联/并联/其他)		6S1P LEDs				

Note:

*6 pcs of LED

*Please consider Allowable Forward Current on used temperature

*6 颗灯

* 请考虑允许范围内的正向电流的使用温度

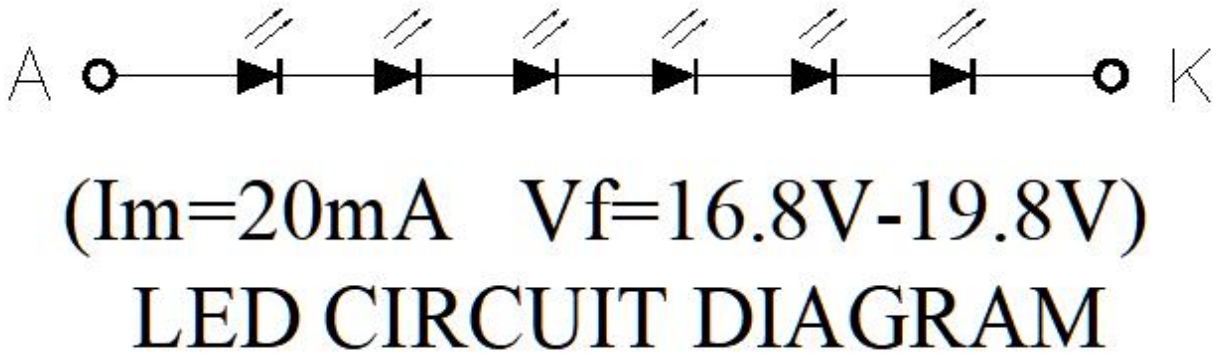


Fig.1*Schematics drawing of lighting （绘制照明图 图.1）

6. Interface signals（接口信号）

TFT Module Interface description（TFT 模块接口描述）

Interface No.	Name	I/O or connect to	Description
1	LEDA	P	Power for LED backlight(Anode)
2	LEDA	P	Power for LED backlight(Anode)
3	NC	/	No connection
4	NC	/	No connection
5	LEDK	P	Power for LED backlight(Cathode)
6	LEDK	P	Power for LED backlight(Cathode)
7	GND	P	Ground
8	GND	P	Ground
9	I2C_DATA	I/O	I2C interface data pin
10	I2C_CLK 3.3V	I/O	I2C interface clock pin
11	LCD_RST	I	External reset for LCD
12	CTP_RST	I/O	External reset for TP
13	GND	P	Ground
14	CTP_INT	I/O	Touch screen interrupt
15	GSENSOR_INT	I/O	Gsensor interrupt
16	GND	P	Ground
17	DSI_CLK_N	I	MIPI-DSI clock lane negative-end input pin
18	DSI_CLK_P	I	MIPI-DSI clock lane positive-end input pin
19	GND	P	Ground
20	DSI_D0_N	I/O	MIPI-DSI data lane negative-end input pin zero
21	DSI_D0_P	I/O	MIPI-DSI data lane positive-end input pin zero
22	GND	P	Ground
23	LCD_DET	O	LCD ID
24	SYS_VCC3V3	P	Power for LCD(3.3V)
25	SYS_VCC3V3	P	Power for LCD(3.3V)

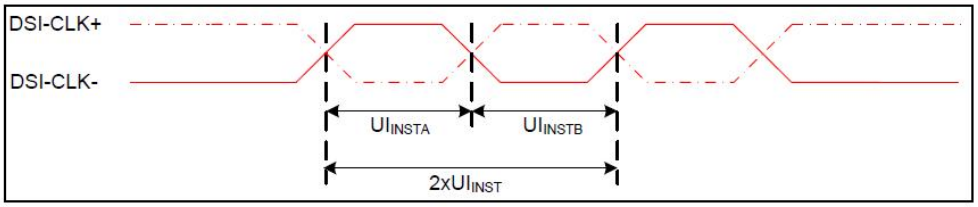
CTP Module Interface description（CTP 模块接口描述）

Interface No.	Name	I/O or connect to	Description
1	I2C_DATA	P	I2C interface data pin
2	I2C_CLK	P	I2C interface clock pin
3	CTP_RST	I/O	External reset for TP
4	GND	I/O	Ground
5	CTP_INT	I/O	Touch screen interrupt
6	LCD_3V3	I	Power for TP 3.3V

7. AC CHARACTERISTICS（交流特性）

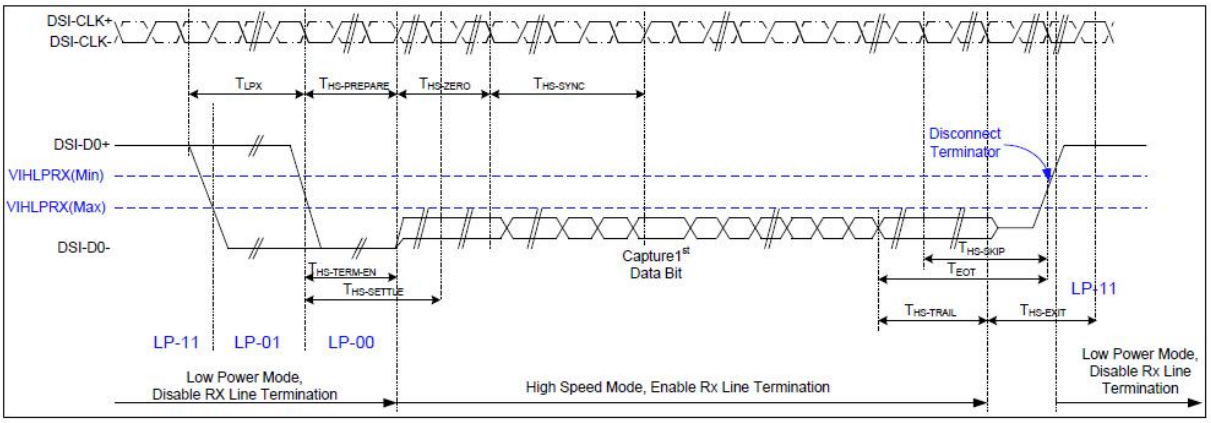
7.4.5 MIPI Interface Characteristics

High Speed Mode – Clock Channel Timing



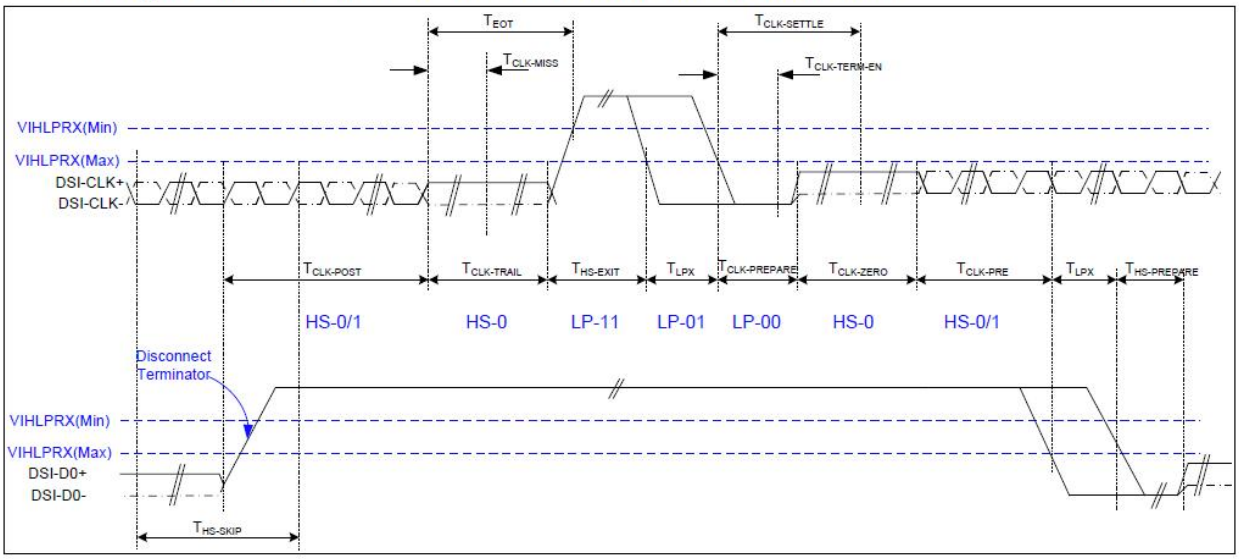
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-DATA_P/N	2xUI INST	Double UI instantaneous	4	25	ns	
DSI-DATA_P/N	UI INSTA ,UI INSTB	UI instantaneous Half	2	12.5	ns	

High-Speed Data Transmission



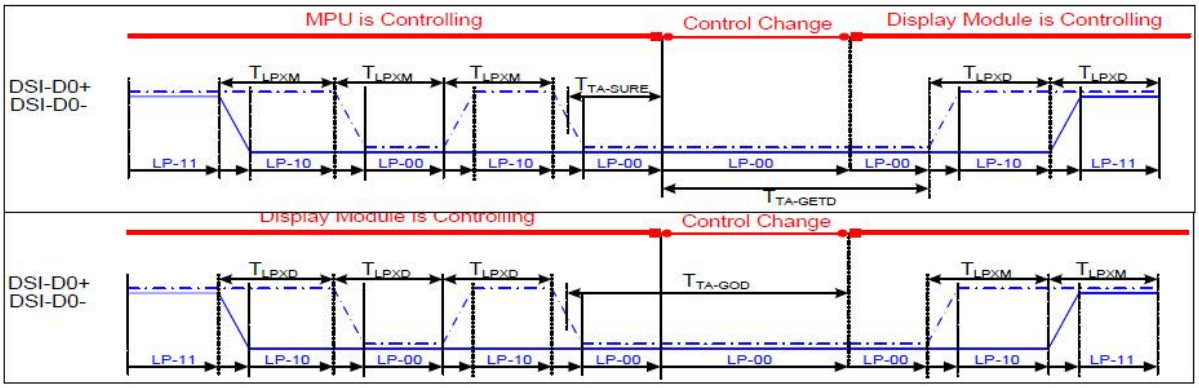
Parameter	Symbol	MIN	TYP	MAX	Unit
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of t HS-TRAIL or t CLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable data receiver line termination measured from when Dn crosses VILMAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode



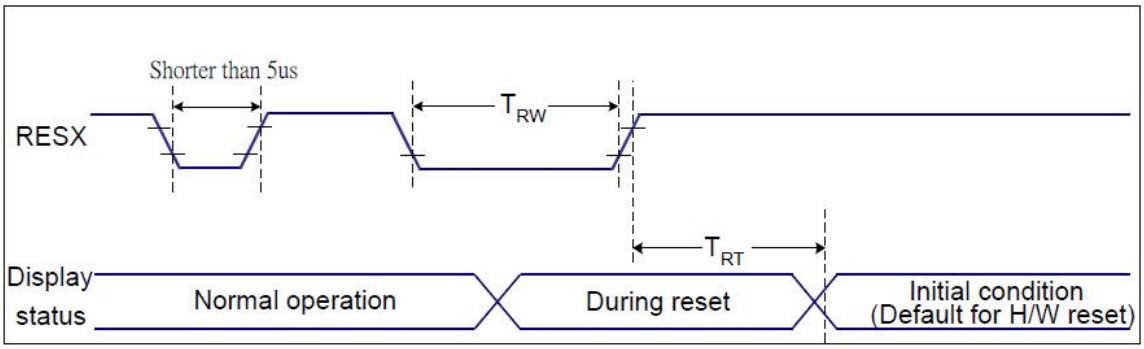
Parameter	Symbol	MIN	TYP	MAX	Unit
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI			ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$			60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38		95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60			ns

Bus Turnaround Procedure



Parameter	Symbol	MIN	TYP	MAX	Unit
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	47.5	50	52.5	ns
Ratio of T_{LPX} (MASTER)/ T_{LPX} (SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		2 T_{LPX}	ns
Time to drive LP-00 by new TX	T_{TA-GET}		5 T_{LPX}		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		4 T_{LPX}		ns

7.4.6 Reset Timing



Reset Timing

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 1 Reset Timing

Notes:

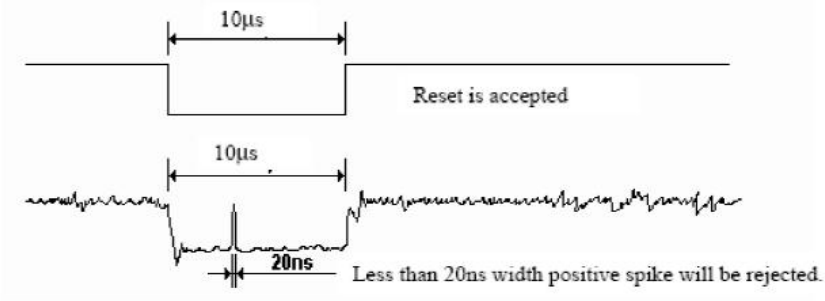
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. POWER SEQUENCE（电源时序）

VDDI and VDD can be applied in any order.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

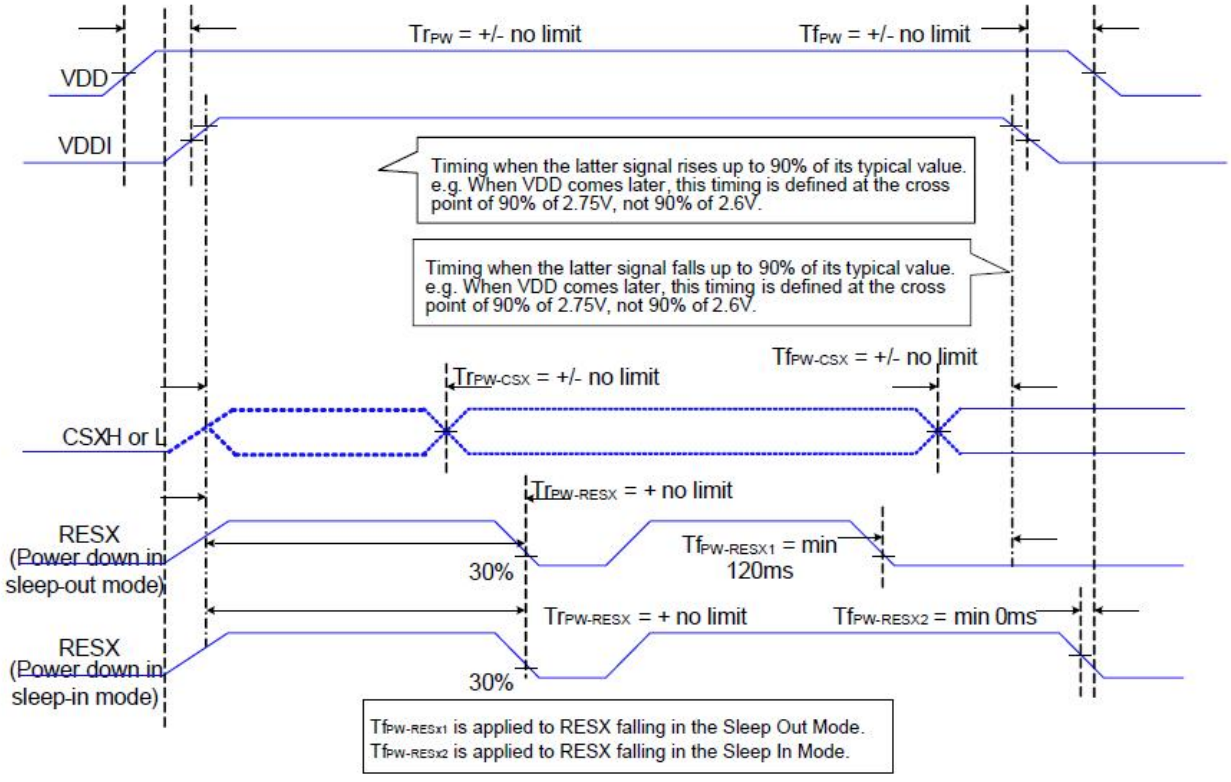
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

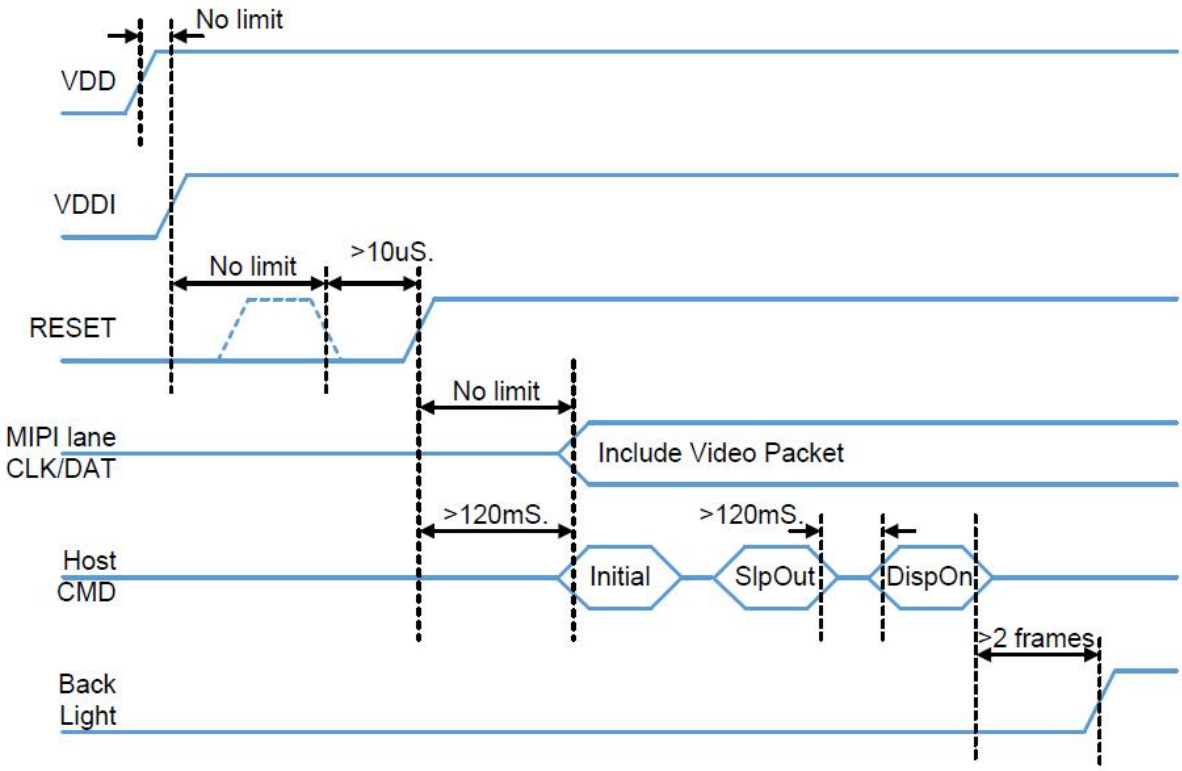
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below (320RGB x 480)



The power on/off sequence is illustrated below for other resolution (less than 320RGB x 480)



9. Optical Characteristics（光学特征）

Item 项目		Symbol（样品）	Condition（条件）	Min.（最小值）	Typ.（标准值）	Max.（最大值）	Unit（单位）	Remark（备注）
Response time（响应时间）	Rise（上升）+Fall（下降）	Tr +Tf	θ=0°	-	30	35	ms	Note 1 FIG.1
Luminance（亮度）		Br	θ=0°	800	850	-	Cd/m^2	Note 3 FIG.2
Luminance uniformity（亮度均匀性）		YU	θ=0°	80	-	-	%	Note 4 FIG.2
Contrast ratio（对比度）		CR	θ=0°	800	1000	-	-	Note 2 FIG.2
Viewing angle(with Polarizer)（视角）	Top（顶部）		CR≥10	80	-	-	degree	Note 6 FIG.3
	Bottom（底部）			80	-	-		
	Left（左边）			80	-	-		
	Right（右边）			80	-	-		
White Chromaticity（白色色度）		X	CIE	0.28	0.31	0.34	-	Note 5 FIG.2 CIE1931
		Y		0.3	0.33	0.36	-	
NTSC（色彩饱和度）			-	60	65	-	%	Note 5 FIG.2

Note1. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state.Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%.

And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

Note2.Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula.

For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

Measured at the center area of the LCD

Note3.Definition of surface luminance

Surface luminance is the luminance with all pixels displaying white.

For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note4.Definition of luminance uniformity

The luminance uniformity in surface luminance is det-ermined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$Yu = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.

For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON's BM-5or BM-7 photo detector or compatible.

FIG.1. The definition of response Time

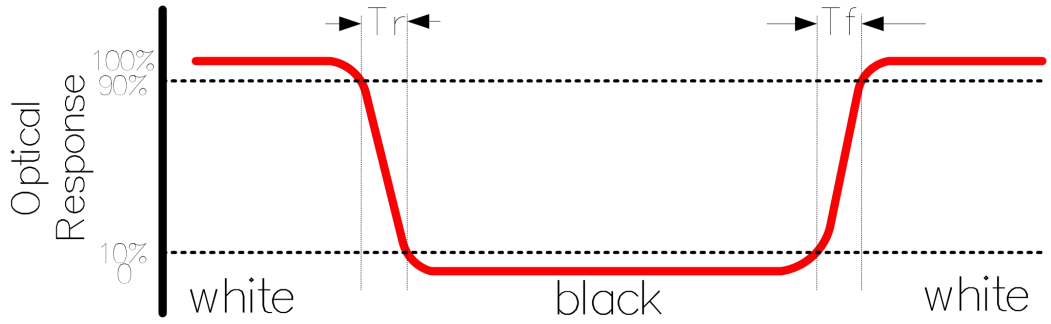


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

H,V : Active area

Light spot size ∅=1.5mm (BM-7)50cm distance or compatible distance from the LCM surface to detector lens.

Test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-7 or compatible ,see Figure b.

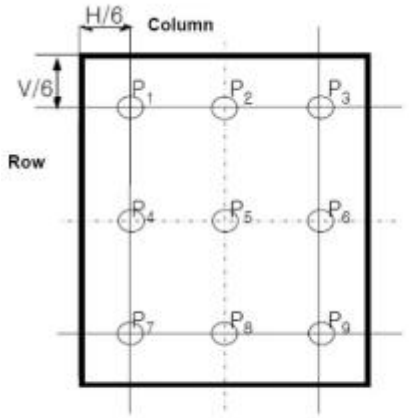


Figure a

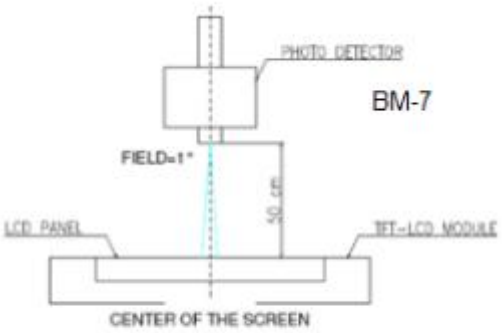
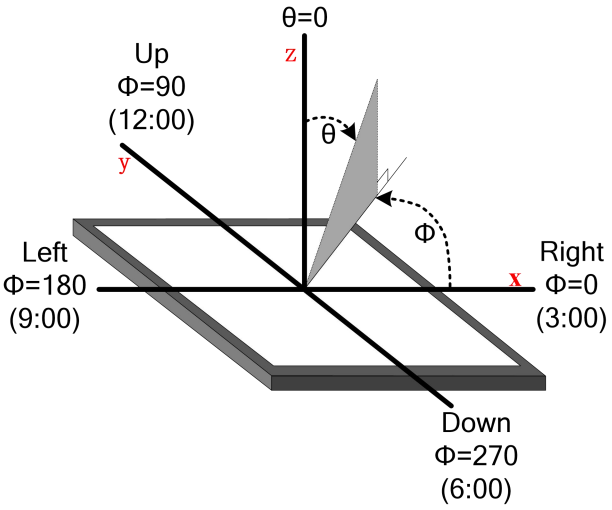
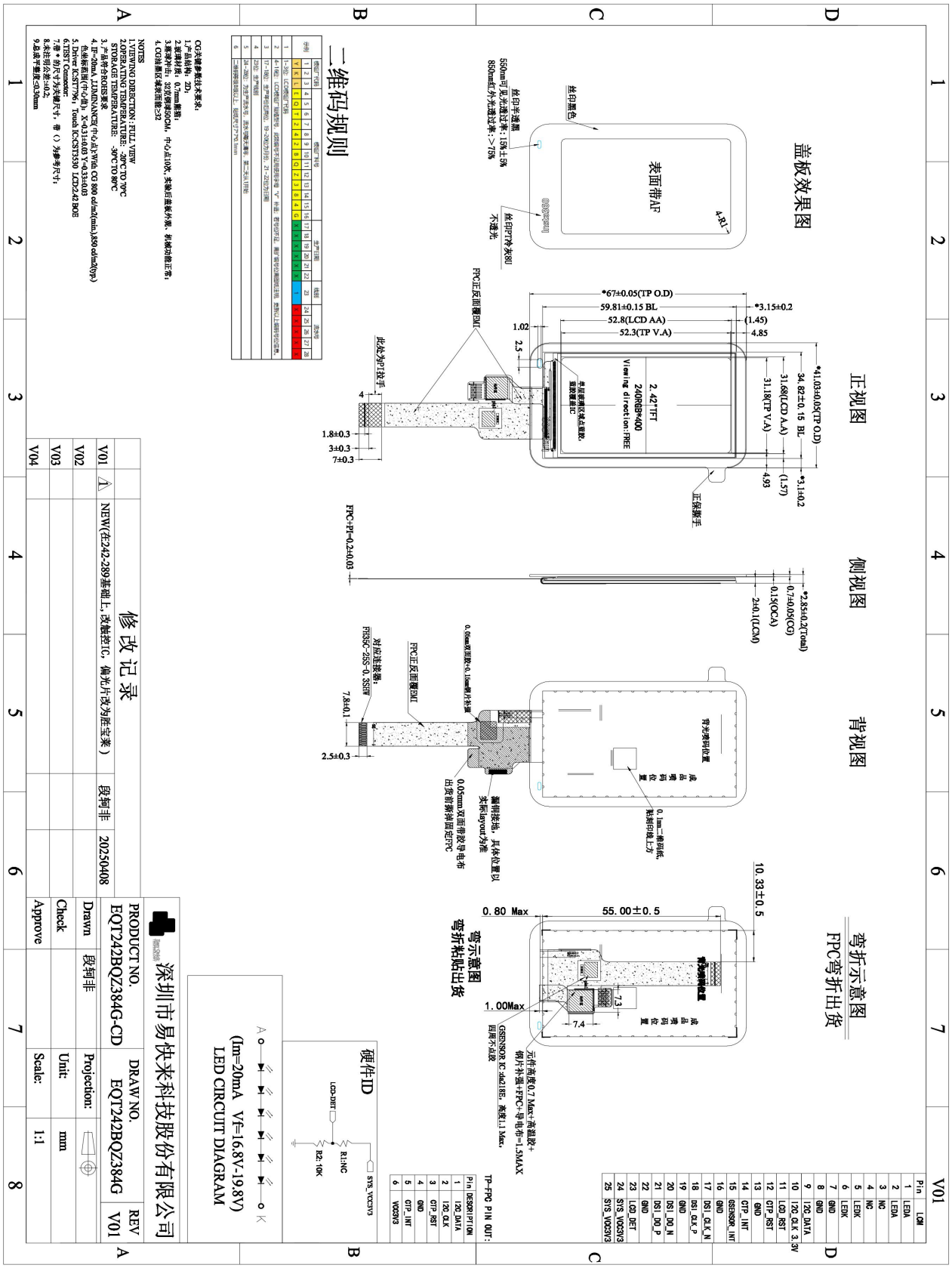


Figure b

FIG.3. The definition of viewing angle



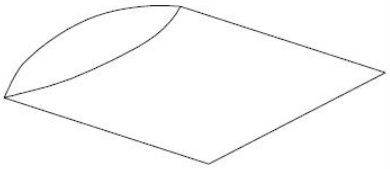
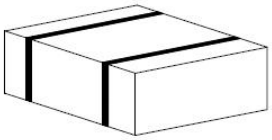
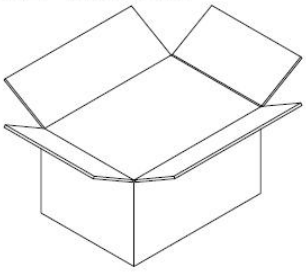
10.LCD Module Outline dimensions （模组外形图 ）



11. Packaging Specification（包装规格）

1.1 Package quantity in one Box : 400 PCS
1.2 Box Size : 380 mm * 330 mm * 210 mm
1.3 1 BOX = 2 CARTON
1.4 1 CARTON = 10 (Full tray) + 1 (dummy / top tray) =11 tray
1.5 1 TRAY = 20 PCS LCM

注：此为示意图

1.将产品放入吸塑盘内，每盘放 X PCS产品 	2.将吸塑盘叠放在一起，N+1(空盘)，两端用胶带固定 	3.将打包好的吸塑放入到包装袋中 
4.将包装袋固定好为一小包，根据客户要求选择是否贴标签 	5.产品装箱，先在纸箱底部放一层纸板，接着放入1包产品，在包装好的产品上再放一层纸板，然后再放入一包打包好的产品，最后盖上一张纸板后封箱 	6.封箱后在外箱侧面贴外箱标签